SILICON DEVICE PERFORMANCE MEASUREMENTS TO SUPPORT TEMPERATURE RANGE ENHANCEMENT

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Prepared by:

James Bromstead
Bennett Weir
R. Wayne Johnson, Principal Investigator
Ray Askew, Principal Investigator

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Auburn University
Center for the Commercial
Development of Space Power
231 Leach Center
Auburn, AL 36849

MCT Testing

The following section deals with the tests which were performed on the MOS controlled thyristor (MCTA60P60). This device is rated for 60A and for an anode to cathode voltage of -600V. All of the tests were performed in the Delta Designs 9023 oven. Tests include gate to anode leakage current, off-state leakage (cathode leakage current), and gate to cathode leakage current. In addition, switching speed tests are planned.

On-State Voltage

The Tektronix 371 curve tracer was used to perform the on-state voltage versus temperature test. The test was conducted with a gate to anode voltage (Vga) of -10V and an on-state current of 60A. The results of the test are shown in Figure 1.

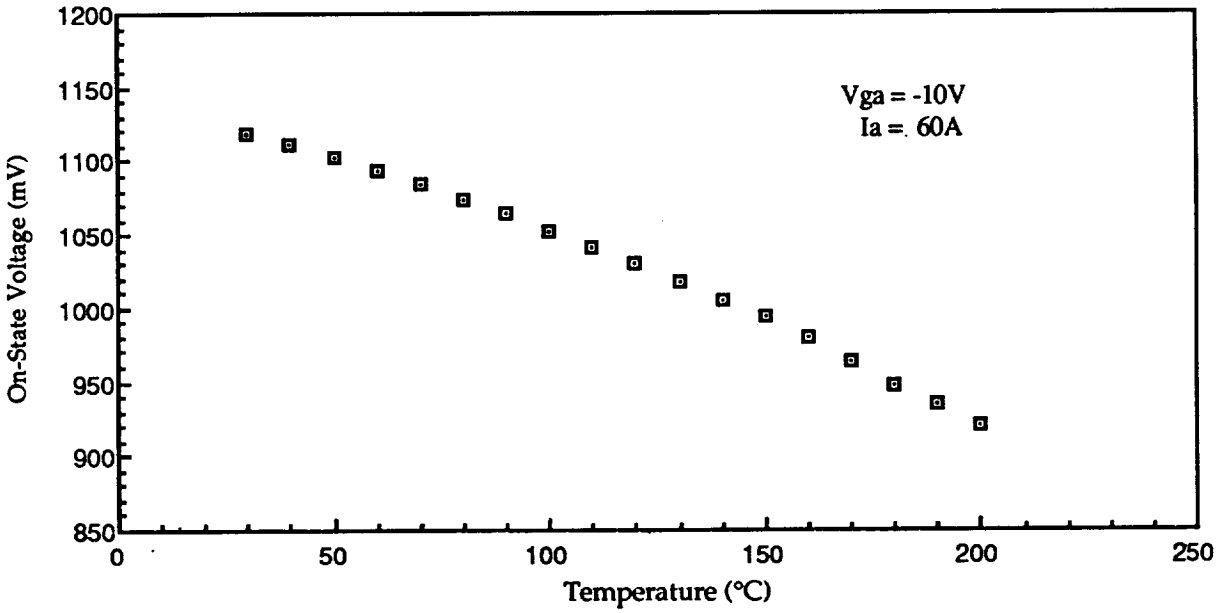

Figure 1. MCT On-State Voltage Versus Temperature.

Gate to Anode Leakage Current

The gate to anode leakage current versus temperature test was done with the gate to anode voltage (Vga) equal to +/-20V and the cathode shorted to the anode. Vga was supplied with the HP6030 power supply and the gate to anode leakage current (Igas) was measure using the DM5120 multimeter. All values over the temperature range 20°C to 190°C were less than 1nA (the resolution limit of the measurement system). However, the Vga=-20V reading at 200°C was 3nA. The measured values were well below the manufacturer's tentative specified maximum

room temperature leakage current of 200nA. The device is not commercialized and the maximum ratings indicate a conservative upper limit.

Off-State Leakage Current

Results of the off-state leakage current versus temperature test are shown in Figure 2. The test was conducted with Vga=10V and Vak=-500V. Vak was supplied by the HP6030 power supply, Vga was supplied by the PS5020 power supply while the cathode current was monitored with the DM5120 multimeter. In this test, the device failed during the 200°C measurement, Figure 2. In order to inspect the failure, the top was removed from the device (MCT #1) and SEM pictures of the damaged areas were taken. Figure 3 shows the gate-anode region of the MCT. Metal from the gate pad bond has been explosively removed, revealing the underlying oxide layer. Terminal characteristics of the device are shown in Figures 4 and 5. The anode to cathode characteristic, shown with the gate terminal open, displays a diode-like response, while the gate to anode (cathode terminal open) response shows an 8.3Ω short.

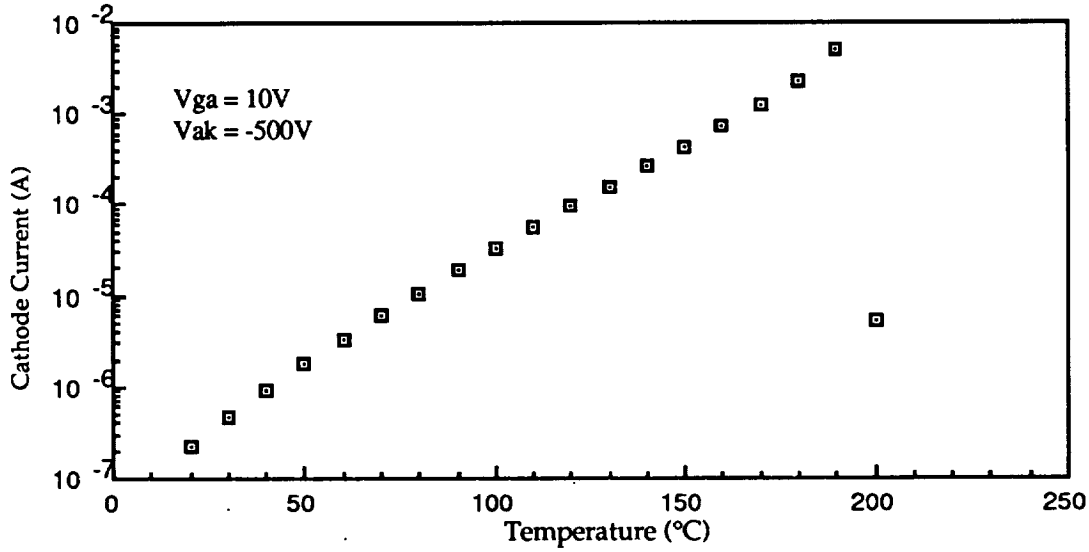

Figure 2. MCT Off-State Leakage Current Versus Temperature.

Gate to Cathode Leakage Current

An additional test was run to measure the gate to cathode leakage current with the gate to cathode voltage (Vgk) held at -500V by the HP6030 power supply, and the anode left open. This test was conducted to investigate the previous failure during off-state leakage measurement, therefore the larger temperature increments were initially used. The gate to cathode leakage current was measured by the DM5120 multimeter. In this test the device to failed during the 140°C measurement. The results of this test are shown in Figure 6. The anode to cathode(gate open) and gate to anode(cathode open) voltage versus current plots for

Figure 3. SEM Picture of MCT #1 Gate Contact Region.

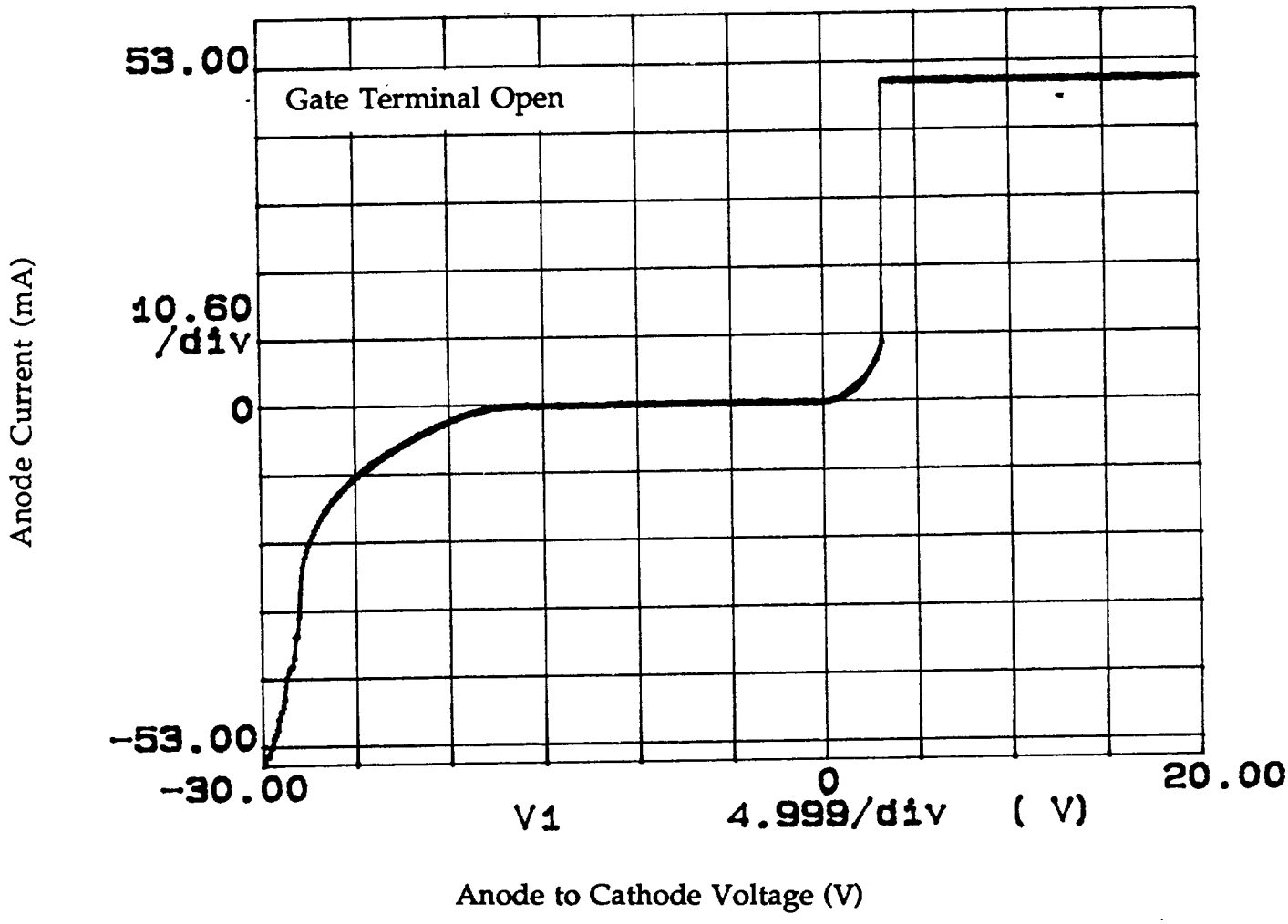

Figure 4. MCT #1 Anode to Cathode Voltage Versus Current (open gate).

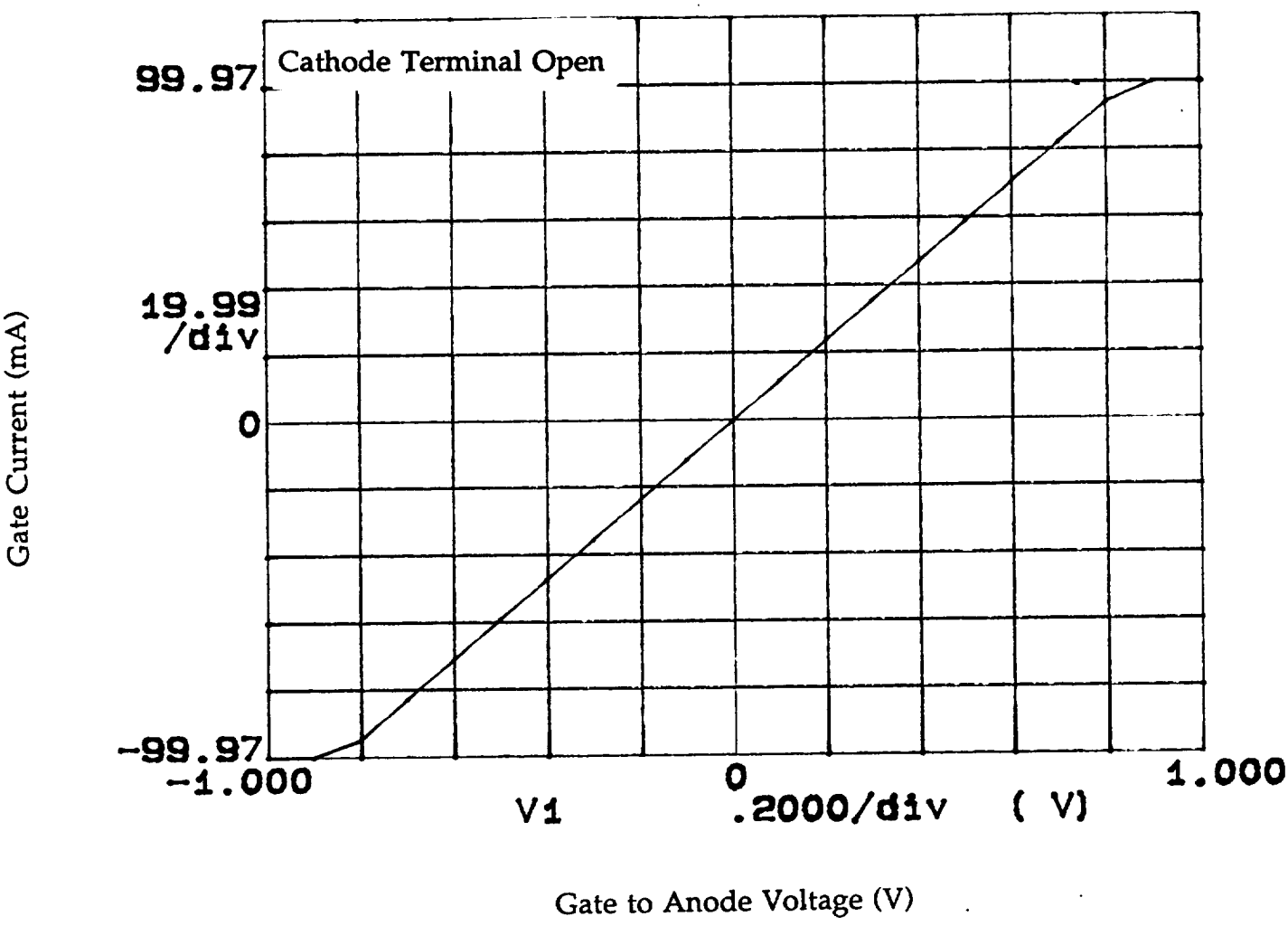

Figure 5. Failed MCT #1 Gate to Anode Voltage Versus Current (open cathode).

the failed device (MCT #2) are shown is Figure 7. and Figure 8. respectively. These responses are very similar to those of the other failed MCT. Further analysis of these failures will be conducted after the switching tests are completed due to the limited number of devices available. This process will be initiated by repeating the leakage current measurements while monitoring all terminal currents.

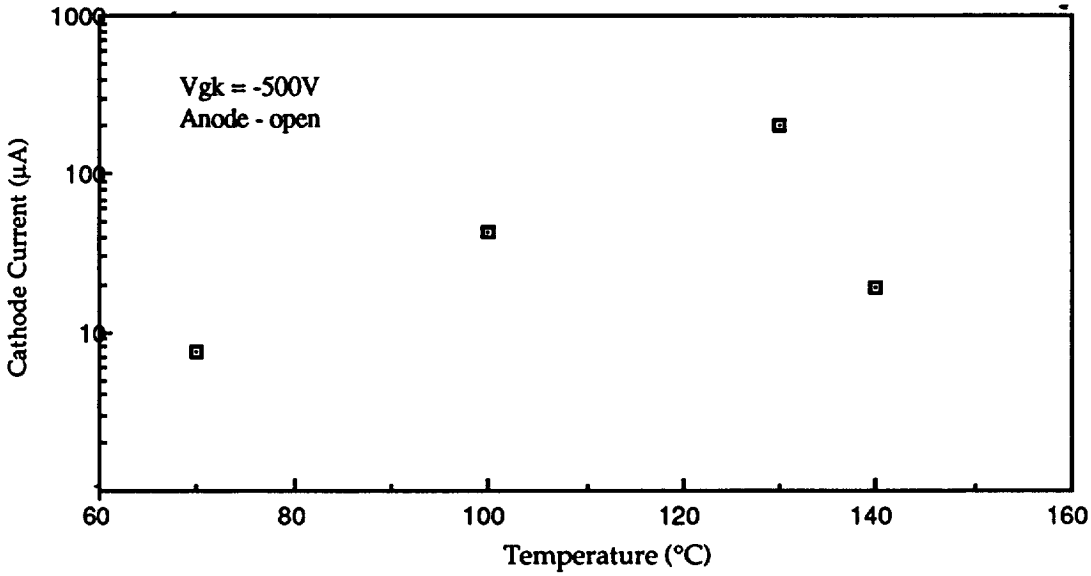

Figure 6. MCT Gate to Cathode Leakage Current Versus Temperature.

DC-DC Switch-Mode Converter

A 28V to 42V boost converter is being designed using the IGBT (TA9876) that was previously characterized, see Appendix A. Figure 9. shows the preliminary design. The converter uses a resonant switch to provide zero-current switching. This is done to lessen the stress on the IGBT during switching and to reduce the switching losses in the IGBT. A Unitrode UC3860 provides the pulse frequency modulated control and the gate drive for the IGBT. The prototype of this converter is operating open loop at room temperature.

Figure 10. shows the inductance change versus temperature of the two cores used in the design (L1 = Magnetics 58867-A2 and L2= Magnetics 58928-A2). These are ferrite cores and will be changed in the next design since ferrites are not space qualified. The 40μF filter capacitor is not a particular problem since its value need not be constant over the temperature range. The 8μF capacitor in the resonant switch however presents a significant problem since it's value must be constant for this control scheme. The 8μF value of the capacitor is necessary because of the current levels of the converter and the losses in the IGBT. In the higher power versions, this capacitor will have to be much higher in value. At this time, the capacitor value has been chosen empirically. As the power level was increased to 100W, the value of the capacitor had to be increased.

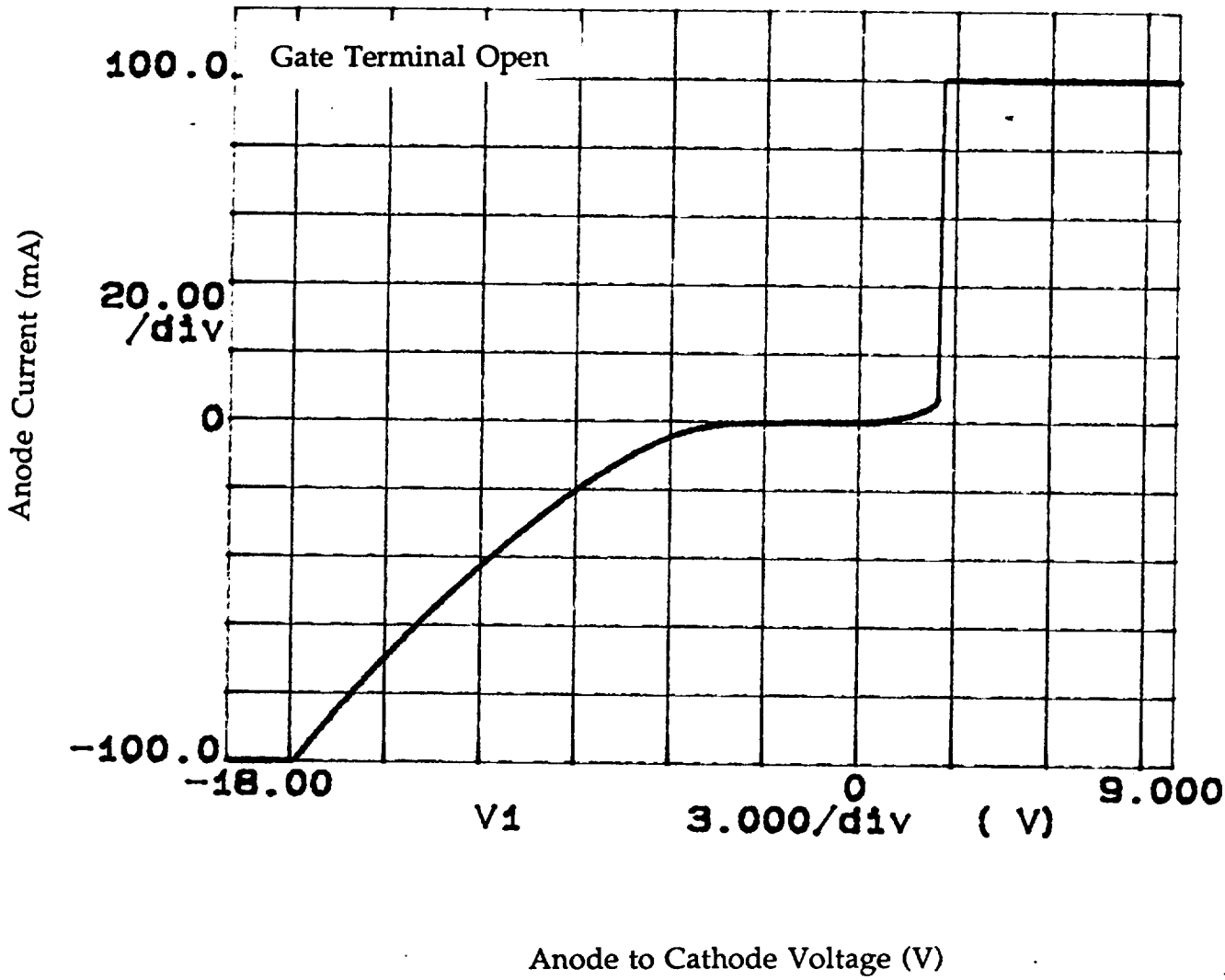

Figure 7. Failed MCT #2 Anode to Cathode Voltage Versus Current (gate open).

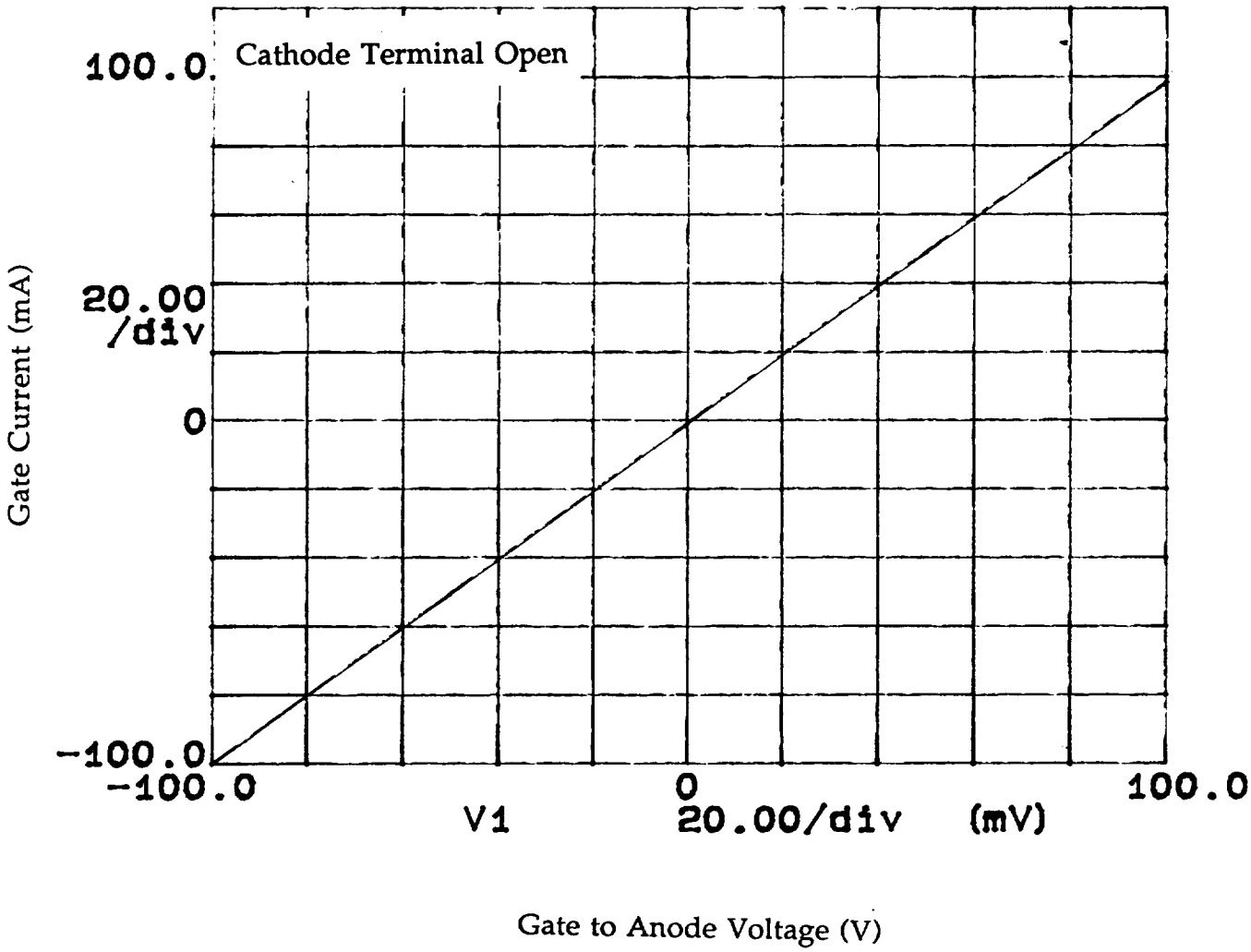

Figure 8. Failed MCT #2 Gate to Anode Voltage Versus Current (cathode open).

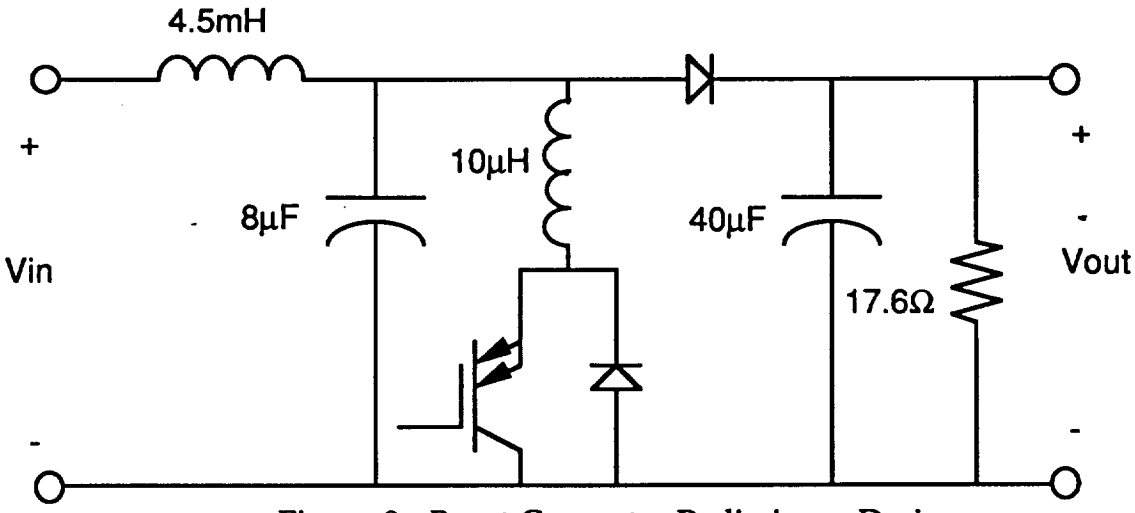

Figure 9. Boost Converter Preliminary Design.

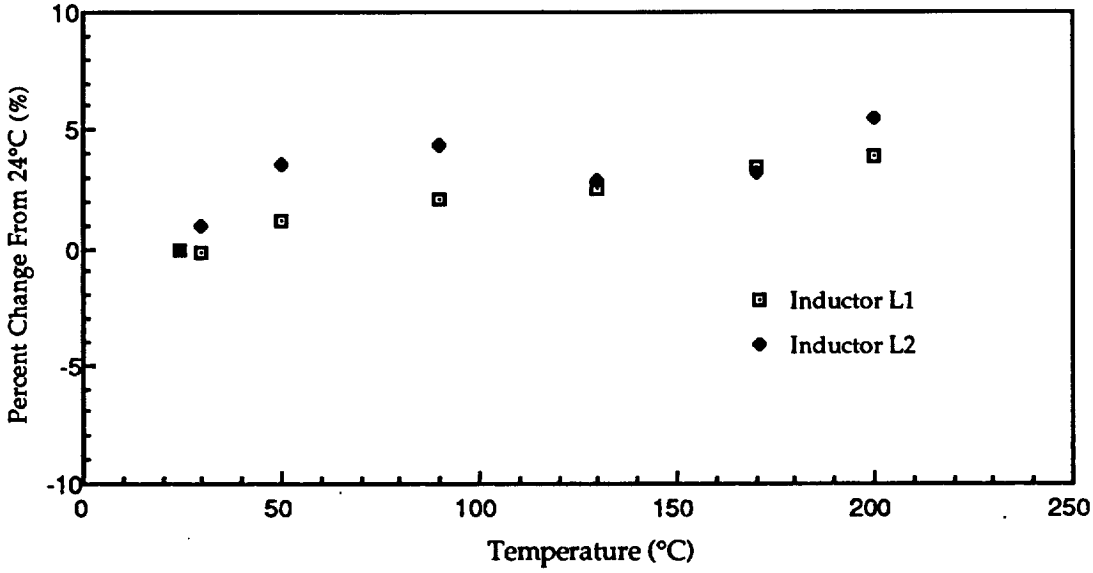

Figure 10. Percent Change In Inductor Value Versus Temperature.

H-Bridge Inverter

As a demonstration vehicle and circuit for life testing, an H-Bridge inverter design was chosen, Figure 11. The inverter test circuit is based on zero voltage switching, using split inductors in each leg of the bridge. These inductors and controlled switching produce a half-wave resonant current pulse through the switching device. Anti-parallel diodes, 1N3891 (12A-200V fast recovery diodes), commutate the attenuated second half-wave

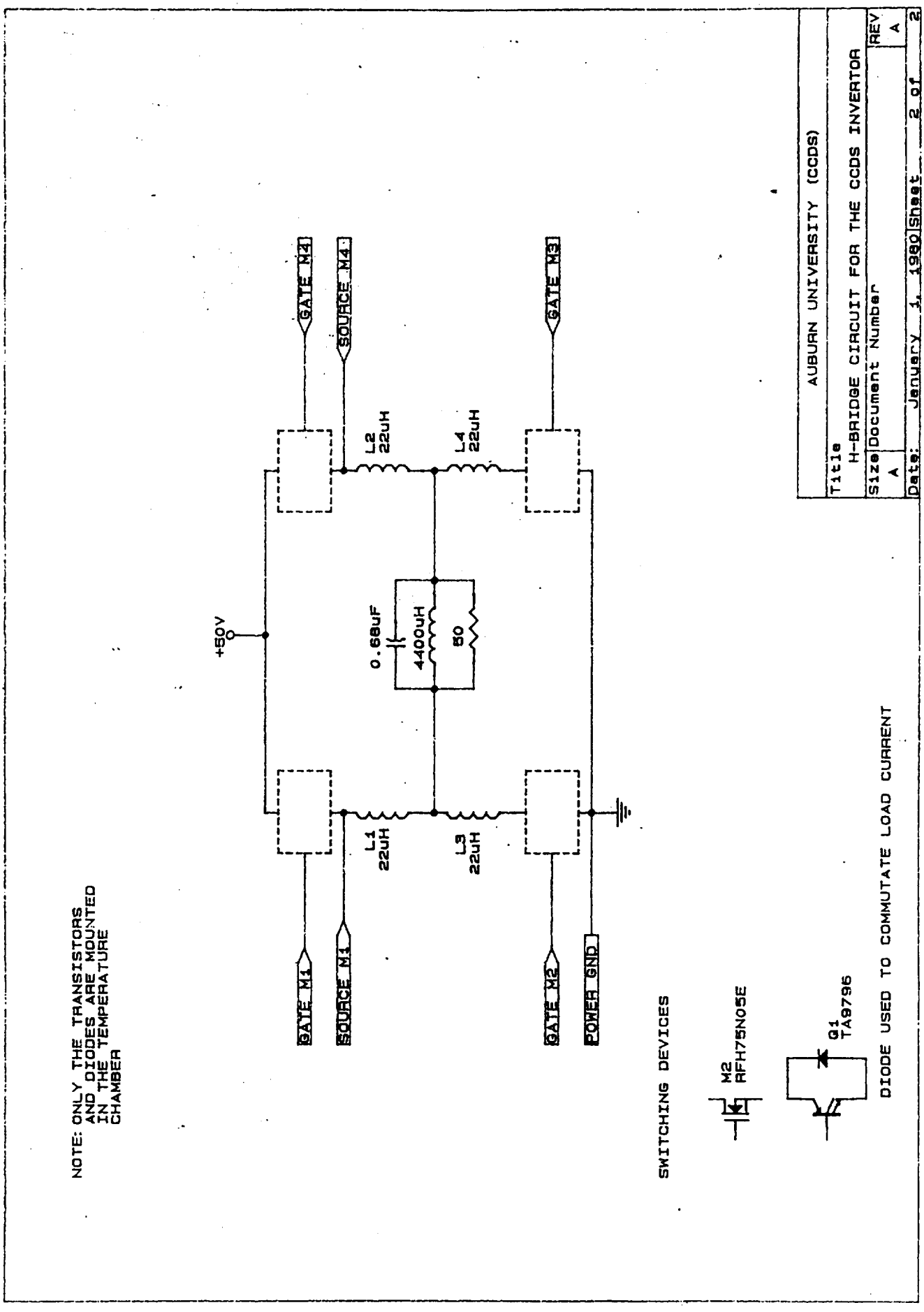

Figure 11. H-Bridge Schematic.

current through the device thus aiding in the turn-off of the device by reducing the reverse voltage across the device. In the case of the MOSFETs, a Schottky diode, MBR3535, was placed in series with the device and the inductor to block the conduction of the FETs slow body diode.

Control of the inverter is generated by a Unitrode UC3860 and International Rectifier IR2110's, Figure 12. The control loop for the inverter is left open in order to reduce circuit complexity. Problems in the earlier versions of the inverter with "Hard" driving of the high-side transistors resulted in ringing of the gate drive signal and destruction of the IR2110 driver have been corrected.

Redesign of the MOSFET (RFH75N05E) and the IGBT (TA9796) versions of the inverter have produced 25A peak device current for the MOSFET converter and 20A peak current in the IGBT. The limit of 25A peak current in the MOSFET version is imposed by the inability of the converter to produce higher device currents while limiting worst case device voltages below the MOSFET's blocking voltage limit of 50V. Also the leads of the TO-3 package are limited to 25-30A. Peak current in the IGBT has been designed at 20A (59% of 34A rating), while limiting the commutating current in the 1N3891 to below 12A.

200°C operation of the converters (only the transistors and diodes are at 200°C) has been demonstrated at the design current and voltage levels. Recent failure of a MOSFET operating at 200°C has not been investigated at this time. The device failed in an 'off' condition. This is unlike earlier failures in which the device failed as uncontrolled, low value, non-linear resistors. Three terminal characteristics of the device will be explored before the device is removed from its package for optical and SEM (scanning electron microscopy) inspection.

Progress with earlier N-MOSFET(RFH75N05E) failure analysis has been impeded. It was thought, as of the last report, that Auger profiling of the device would be completed. This device failed with the I-V characteristics shown in Figure 13. It is believed that aluminum diffused through the junction shorting the device during a high current transient. The slow sputter etching rate of the Auger system (10-100A/min) and the time limitations on the system have made depth profiling impractical. Etching the SiO_2 passivation layer and the top aluminum have not been attempted due to the difficult nature of the etching process.

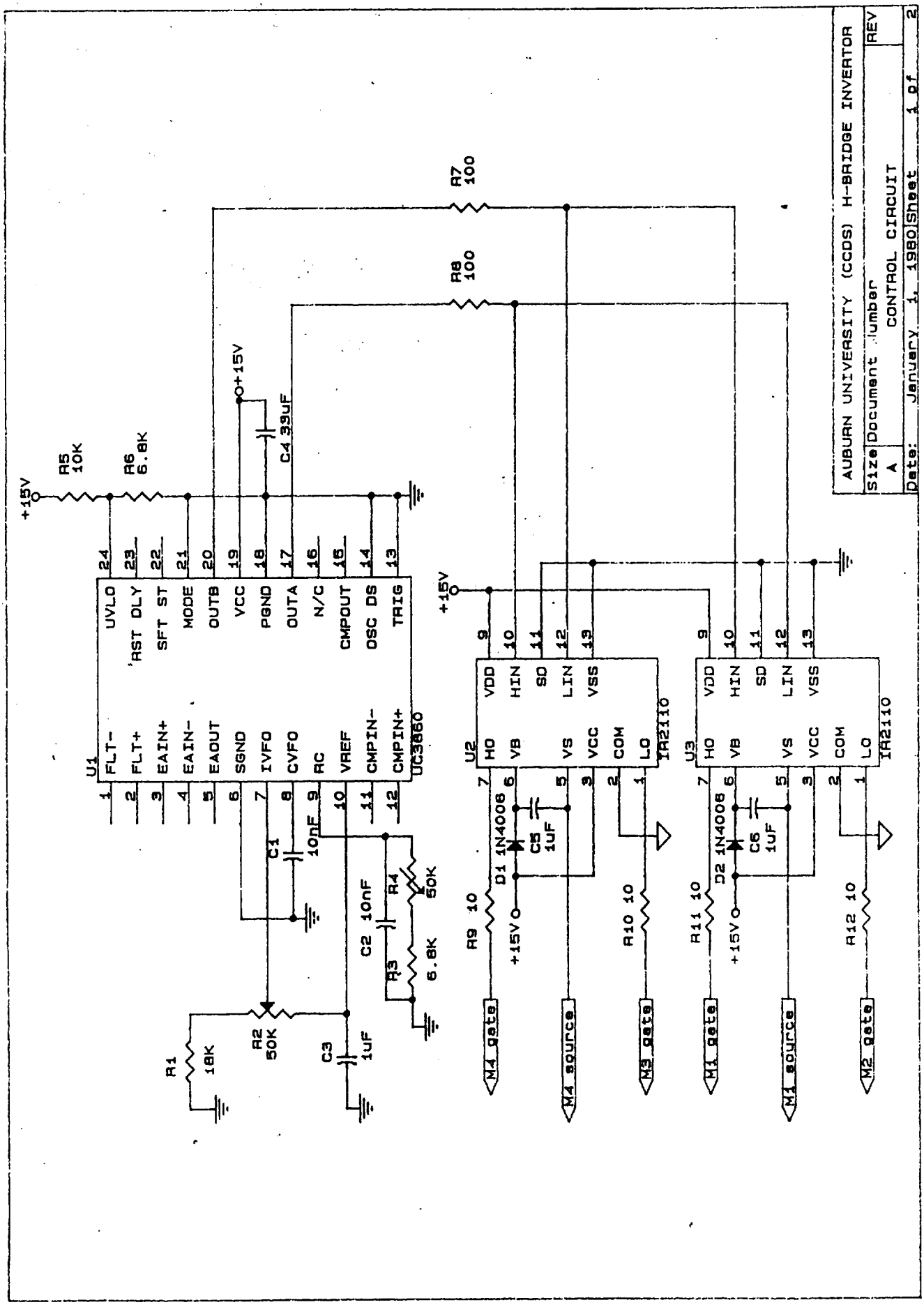

Figure 12. H-Bridge control circuitry.

Conclusions

Testing of the MCT has uncovered a failure mechanism at elevated temperature. The failure appears to be due to breakdown of the gate oxide. Further testing is underway to verify the failure mode.

Higher current level inverters have been built to demonstrate 200°C operation of the N-MOSFETs and IGBTs and for life testing. One MOSFET failed early in testing. The origin of this failure is being studied. No IGBTs have failed.

A prototype 28V-to42V converter has been built and is being tested at room temperature. The control loop is being finalized. Temperature stable, high value (10μF) capacitors appear to be the limiting factor in the design at this time. In this application, the efficiency will be lower for the IGBT version due to the large V_{cesat} (3.5-4V) compared to the input voltage of 28V. The MOSFET version should have higher efficiency; however, the MOSFET does not appear to be as robust at 200°C. Both versions will be built for comparison.

Appendix A

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Semi-Annual Report
May 7, 1991 - November 9, 1991

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December 2, 1991

Auburn University
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INTRODUCTION

This report details the efforts made since the last report was issued. The results of the NPN bipolar transistor (BJT) (2N6023) breakdown voltage measurements have been analyzed. Switching measurement have been made on the NPN BJT, the insulated gate bipolar transistor (IGBT) (TA9796) and the N-channel metal-oxide-semiconductor field effect transistor (MOSFET) (RFH75N05E). Efforts have also been made to build an H-bridge inverter. Also discussed in this report are the plans that have been made to do life-testing on the devices, to build an inductive switching test circuit and to build a dc/dc switched mode converter.

BJT BREAKDOWN VOLTAGE

Figure 1. shows the results from the BJT breakdown measurements. Breakdown voltage in a power device is determined to a first order by the doping concentration in the epitaxial layer and increases in the mean free path. This relation is demonstrated by the equation below. The figure shows an expected initial increase in breakdown voltage with temperature (about 5% per 100°C), with a sudden decrease in breakdown voltage after 150°C.

$$V_{br} = \frac{\varepsilon}{2q} \frac{E_{br}^2}{N_{epi}}$$

This curve was typical of several devices tested. Analysis of this phenomenon concluded increases in both the internal base resistance and base-emitter leakage currents were creating an internal base emitter voltage which begins to turn the device on. The breakdown voltage at 200°C is approximately 10% below the value at 25°C and should not limit designs.

SWITCHING MEASUREMENTS

The major area of work since the last report has been switching tests on the N-MOSFET, BJT and IGBT. Problems in drive circuitry and resistive power loads have greatly delayed these tests.

As with the previous tests, only the heat sink mounted device was placed in the test chamber. This configuration introduced large lead inductances. Even with twisted pairs for the gate/base drive and supply/load leads, ringing persisted in the output due to lead inductances. A major concern was the reduction of these inductances to minimize the ringing.

The evolution of the switching test drive circuit is shown in Figure 2. The first circuit was fabricated as a chip and wire hybrid and placed with the device in the test chamber to reduce the drive lead inductances. This drive circuit was later abandoned due to insufficient current from the totem pole output to drive the MOSFET and IGBT. The next drive circuit tested uses the IR2110 High Voltage MOSFET gate driver. This circuit proved the fastest means of switching the N-MOSFET. The third circuit, although slower, provided the higher current drive needed for the BJT and proved adequate for the IGBT.

Problems persisted in the construction of a purely resistive load. In its final form the load consisted of a parallel combination of 10 Ω, 7 W composite power resistors which were placed in the test chamber with the device. This produced loads with a low temperature coefficient of resistance (TCR), but sizable inductances (R_L=0.67Ω L_L=0.121μH and R_L=5.56 Ω L_L=1.21μH as measured by an HP 4275A Multi-frequency LCR Meter at 10MHz).

Testing was performed by mounting the device and load in a Delta Design 9023 test chamber. Twisted pair leads (<8 inch) connected the device to the gate/base drive circuit (driven by the Tektronics AFG5101 Arbitrary Function Generator) and the load to the voltage supply (HP6032 Power supply). Output waveforms were captured using a Tektronics 2440 oscilloscope, AM503 current amp with A6303 current probe and HC1000 color plotter. Between each test the heat sink and device were allowed to settle to the ambient chamber temperature. Tests were preformed using 100μsec pulses to avoid junction heating

Figures 3-6 show typical N-MOSFET turn-off and turn-on waveforms at 20°C and 200°C, for a V_{DS} = 30V, I_D = 45A (Channel 1 - drain-source voltage @5V/Div, Channel 2 - drain current @10A/Div). Ringing in the turn-off voltage, Figures 3 and 5, waveforms was a result of natural oscillation between the R, L of the load and the C_{gd} of the FET. A 25 Ω gate resistor reduced the ringing in the output, but increased rise and fall times. The graph

of switching time versus temperature, Figure 7, shows an almost flat response to temperature, but with switching time much higher than specified by the manufacturer. The 0.67Ω load used in the test has a time constant, t_{RL} = 316ns, which results in a 10-90% time of 694ns. This value contributed heavily to our room temperature V_{DS} fall time of 620ns which is an order of magnitude longer than the manufacturer's specified typical fall time of 17ns.

In addition to the RL time constant of the load, drive limitations of the IR2110 and the charge-transfer characteristics of the RFH75N05E also contribute to the slow switching times.

As in most FETs the input impedance of a power MOSFET consists of a high input resistance in parallel with an equivalent input capacitance, consisting of the gate to source, C_{gs}, and the gate to drain capacitance, C_{gd}. Due to the Miller effect on C_{gd}, the input capacitance of the MOSFET is not well-defined. The effects of the change in the input capacitance can be seen in the charge transfer characteristic of the RFH75N05E MOSFET, Figure 8, the normalized V_{GS} voltages and corresponding V_{DS} voltages for the FET.

Each of the V_{GS} curves can be viewed as three separate regions of turn-on or turn-off operation. In the first region of turn-on, the V_{GS} curve is linear, the gate voltage has risen to a level where there is drain current conduction. During this period, the gate potential is in the pre-threshold region, and charging the equivalent input capacitance, C_{gd}, thus the slope is fairly constant. The rate of charging in this first region directly affects the turn-on delay. In the second region, turn-on is complete when the drain voltage has switched 90%. There is an abrupt increase in the input capacitance, identified by the flattening of the gate-voltage curve. As the MOSFET turns on, the Miller effect becomes more dominant. C_{gd}, and C_{gs} being depletion-dependant are thus voltage-dependant and change rapidly in this region. In the third region, since C_{gd} is depletion dependant, its capacitance rises dramatically as the voltage between drain and gate diminishes, and changes polarity when V_{DS} drops below V_{GS}. As C_{gd} rises, the Miller capacitance increases even more rapidly, despite the decrease in voltage gain (dV_{DS}/dV_{GS}). The increasing Miller capacitance keeps the gate-voltage characteristic nearly flat until V_{SAT} is reached. After the V_{DS} voltage has decayed to V_{SAT}, the gate then resumes its rise to the imposed gate drive level.

Figures 9-12 show typical BJT turn-off and turn on waveforms, for a V_{CE} = 30V and I_C = 45A. Again ringing in the turn-off voltage, Figures 9 and 11, is due to the inductive load. The maximum specified rise time for the 2N6032 is 1μs and the maximum specified fall time is also 1μs. The values measured at 20°C, V_{CE} rise time of 180ns and a V_{CE} fall time of 120ns, fall well within the maximums specified by the manufacturer. A graph of the change in switching times for the BJT, Figure 13, indicates a fairly flat response in the turn-off voltage and the turn-on current. Most notable in the figure is a 5.59 ns/°C increase in the BJT turn-off current and turn on voltage times. This rate of increase is noted in the turn-off current after 150°C.

Figures 14-17 show the IGBT turn-off and turn-on waveforms at 20°C and 200°C, for a V_{DS} = 150V, I_C = 30A. Ringing in the turn-off voltage waveforms is again a result of the inductive load. A rise time of 250ns and a fall time of 1.214μs were measured for V_{CE} at 20°C. The measured fall time is less than the specified typical value of 1.8μs. The time constant for the 5.56Ω load used is 0.218μs which results in a 10-90% time of 0.479μs. This indicates that the load and temperature do not contribute to the measured times, as shown in Figure 18.

Figures 7, 13 and 18 show a graphical representation of the rise and fall times for the devices. These graphs show a fairly flat response of switching time over the 20°C to 200°C operating temperature. Because the rise and fall times were relatively unaffected by temperature in this switching test it can be seen that all the devices tested still switched at useful speeds even at 200°C.

H-BRIDGE CONVERTER

As part of the lifetime testing, an H-Bridge converter has been designed and built, Figures 19 and 20. With an operating frequency of ~21.5kHz and parallel resonant load, the inverter offered a design in which both the N-MOSFET and IGBT could be used as the switching elements. A problem encountered in the testing the MOSFET version of the inverter has been feedback between the H-Bridge and the gate driver circuitry.

"Hard" driving of the high-side transistors caused coupling of the high voltage power supply with the driver power supply through the same "Miller effect" capacitance found in the MOSFET switching tests. This coupling resulted in ringing on the +15V line. The ringing in the +15V supply line

created changes in the UC3860's V_{REF} and I_{VFO}, resulting in changes in the frequency and width of the UC3860's alternating drive pulses. This led to failures in the IR2110 high-side drivers. Increasing the bypass capacitance on the +15V line did not help with the oscillation. As a solution to this problem the voltage supplies of the UC3860 and IR2110s have been separated. Reducing the IR2110 supply to +14V has also helped to reduce ringing in the gate drive.

Figures 21-24 show operating waveforms of the MOSFET inverter at 20°C. Figures 21 and 22 show the drain-source voltage, V_{DS}, (Channel 1- 20V/Div) and gate-source voltage, V_{GS}, (Channel 2 -10V/Div) of M3, a low-side device, and M4, a high-side device, respectively. Due to the limitation in rated drain-source voltage of the RFH75N05E to 50V, (M4 ~45V), the peak V_{DS} limited the operation of the inverter to a peak device drain current, I_D, of 5.8A. Reduction in the load resistance will allow operation at increase current by reducing the load voltage. The V_{DS} and I_D, of the low-side device M3 are shown in Figure 23, (Channel 1- 20V/Div, Channel 2- 2A/Div), note the commutation of current through the MOSFETs body diode. In our configuration, the natural frequency of the RLC load can be seen to be higher than the inverter switching frequency, thus the diode current should be commutated by the companion FET in the totem pole. But due to the split inductor configuration, the diode current is commutated in the opposing part of the totem pole, and diode recovery problems at higher current will occur. Detail of the forward conduction of the body diode is shown in Figure 24. To remedy the commutation problem the circuit is being reconfigured with a Schottky diode (MBR3535) added in series with each FET and a fast recovery diode (1N3891) in parallel with each FET/Schottky combination as the free-wheeling diode. Reverse current now will then flow through the fast recovery diode, and because of the fast reverse recovery nature of the diode, the current during recovery will be reduced. In the IGBT version of the inverter, the free-wheeling diode is also necessary.

FUTURE PLANS

Life-Testing

Life-testing will be accomplished by running the devices in the configuration detailed in the section on the H-bridge inverter. An inductive switching test will also be performed on the devices. A test circuit will be designed.

Failure Analysis

Failure analysis has begun with N-MOSFET that failed under testing, Figure 25. This device no longer responses to gate drive and produces a resistive I-V characteristic on the curve tracer. It is thought that the source metalization has "punched through" to the drain. After the passivation layer of SiO_2 and source aluminum have been etched and the source-channel will be Argon sputter-etched in an Auger system to profile the elemental content of the junction.

DC/DC Switch Mode Converter

Plans have been made to design a dc/dc switched mode converter. Figure 26. shows the flyback converter configuration which has been selected as the basic converter topology. The design will be implemented using IGBT's and will convert 18V to 120V at a power level of 100W.

Thick film hybrid technology will be used to construct the control circuitry. The materials used in thick films are processed in excess of 800°C and are very stable at 200°C. LM555's are currently being considered for use in the control circuit and will soon be characterized at elevated temperatures.

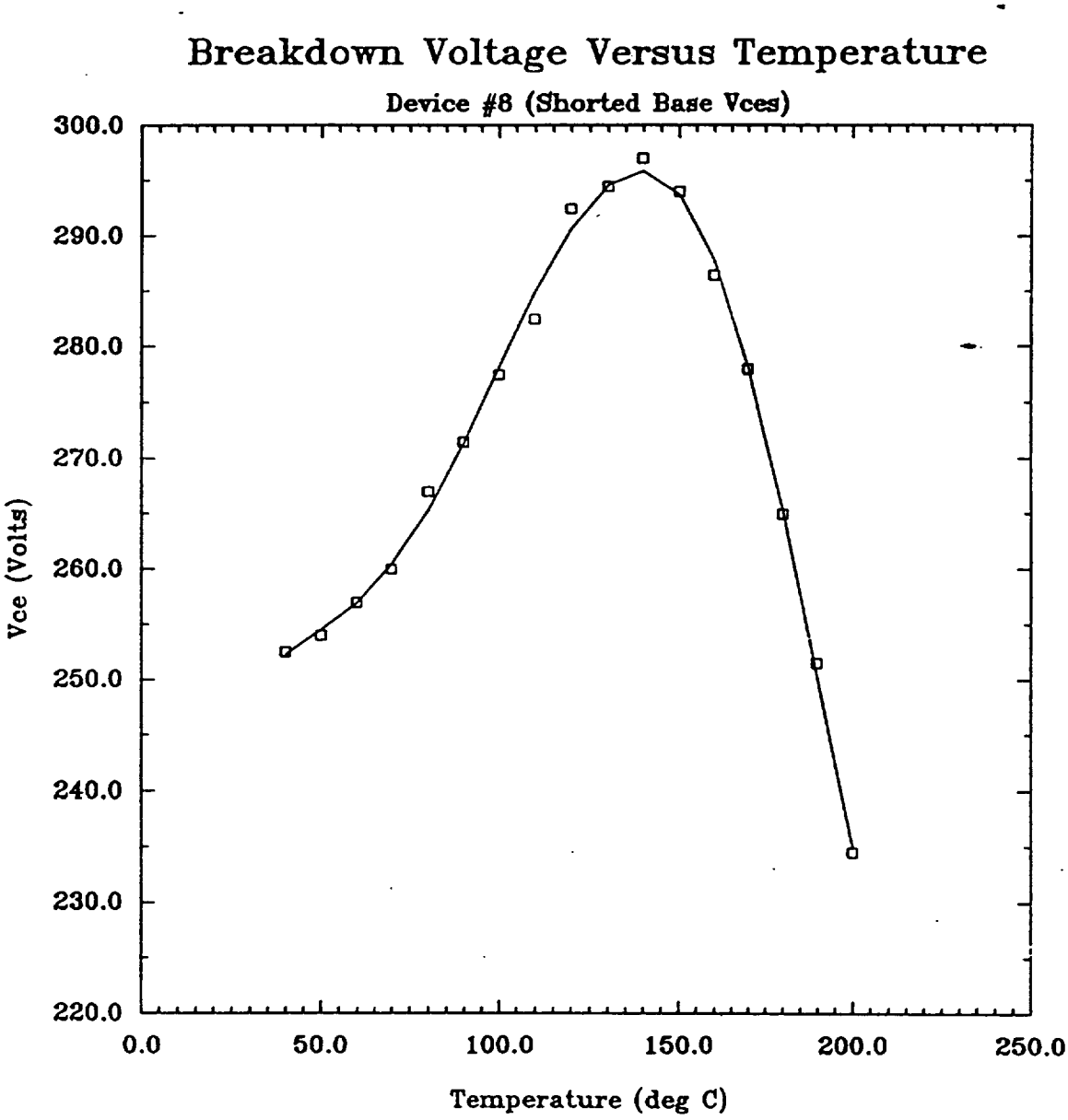

Figure 1. BJT breakdown voltage.

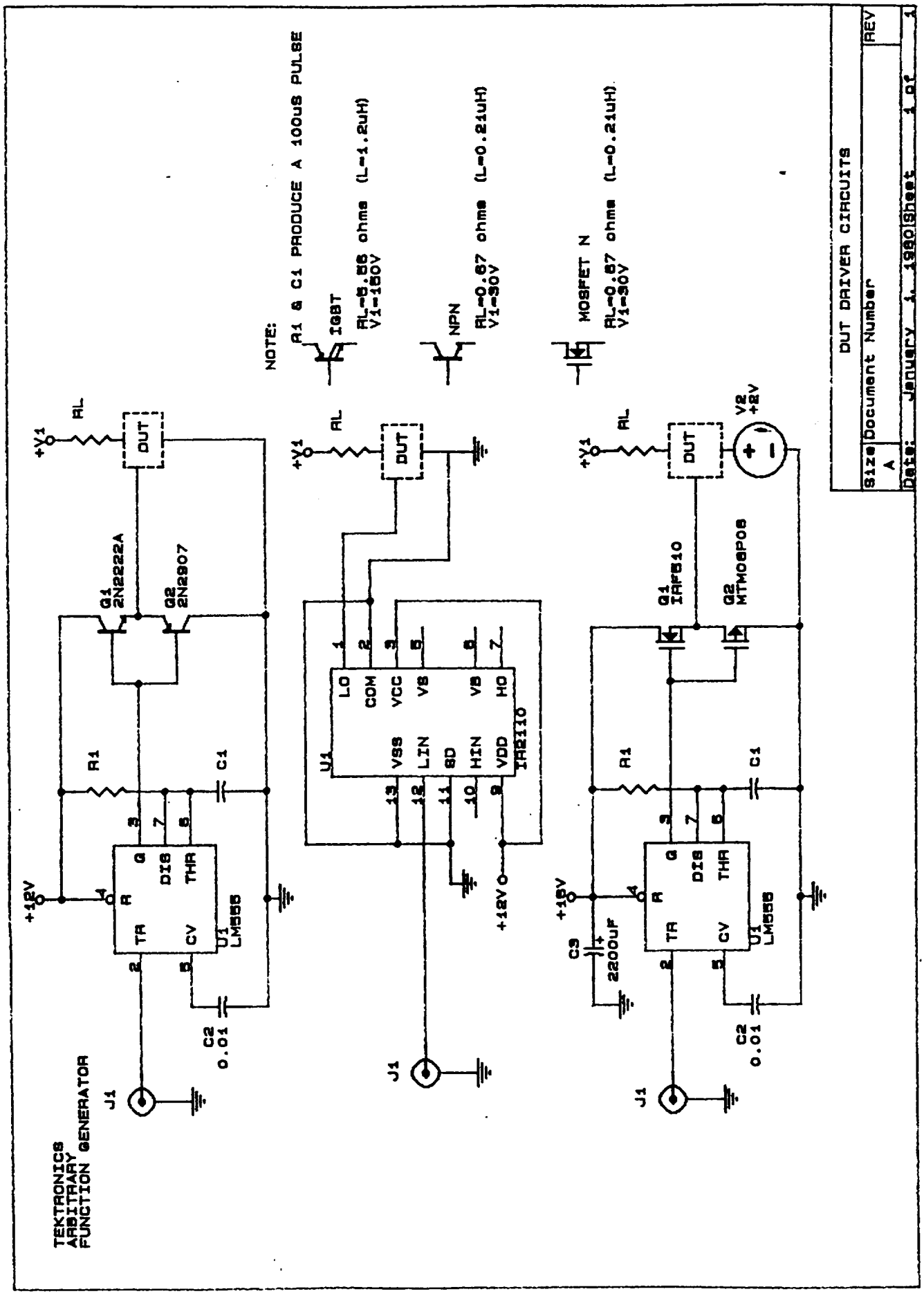

Figure 2. Driver circuits.

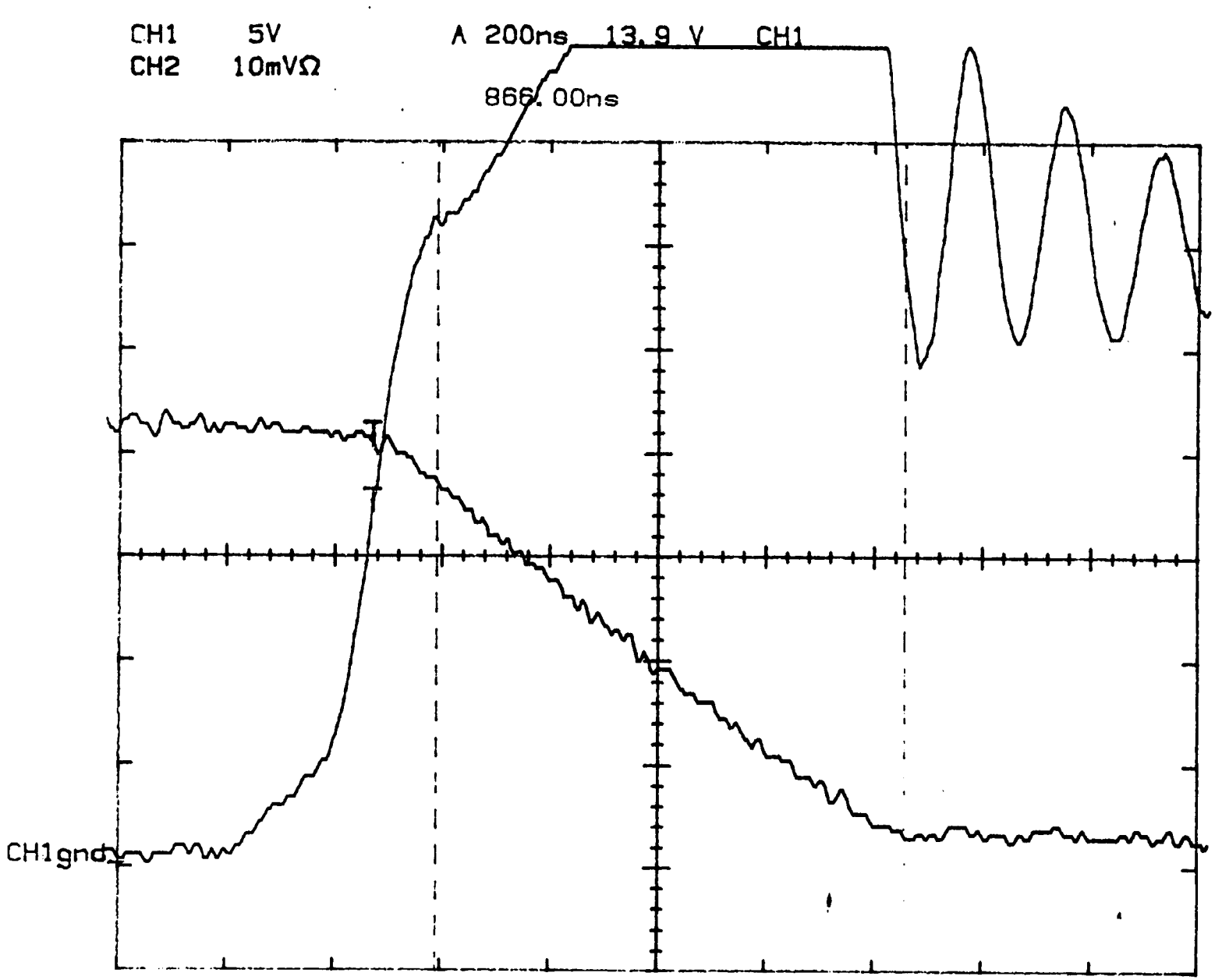

Figure 3. N-channel MOSFET turn off at 20°C.

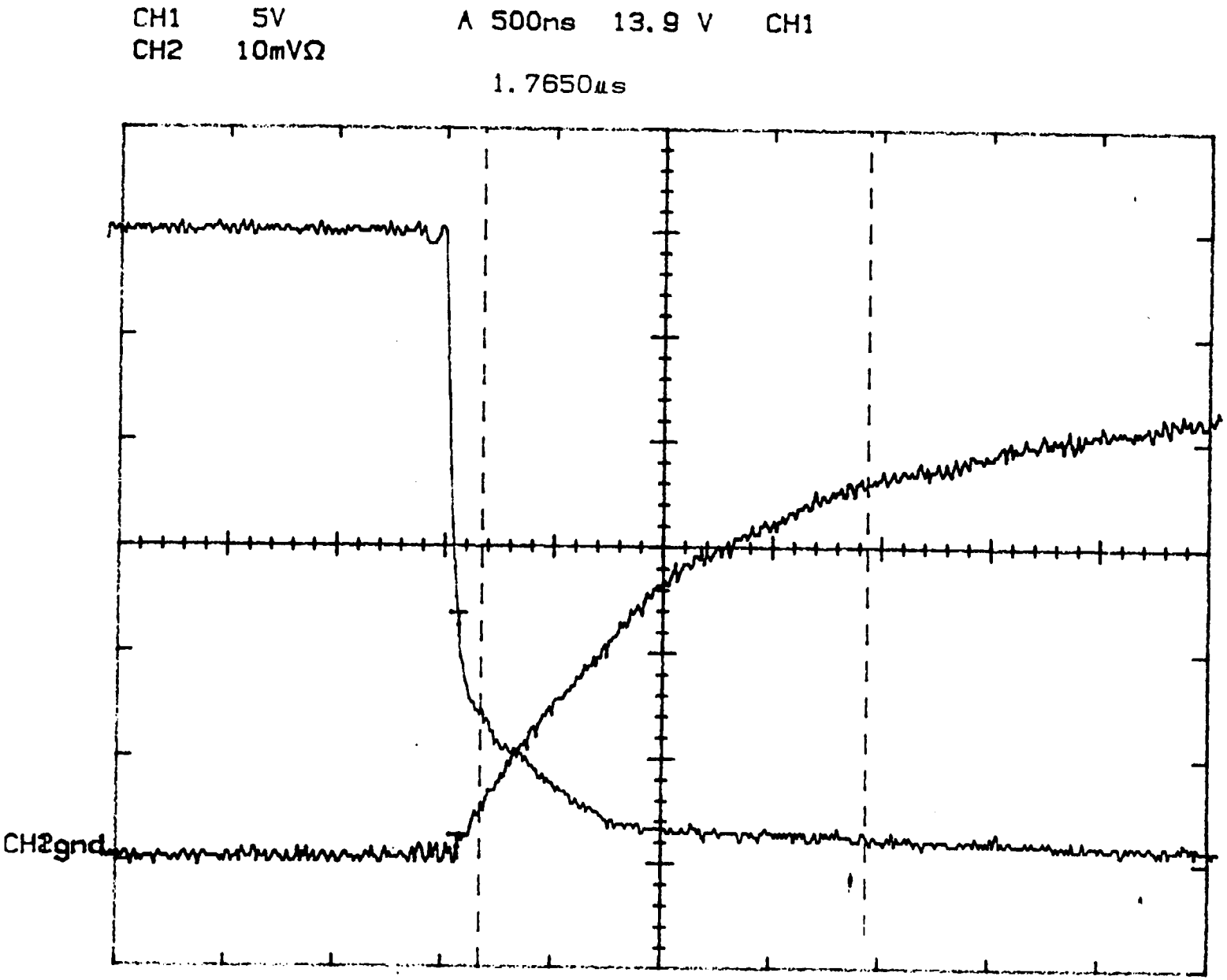

Figure 4. N-channel MOSFET turn on at 20°C.

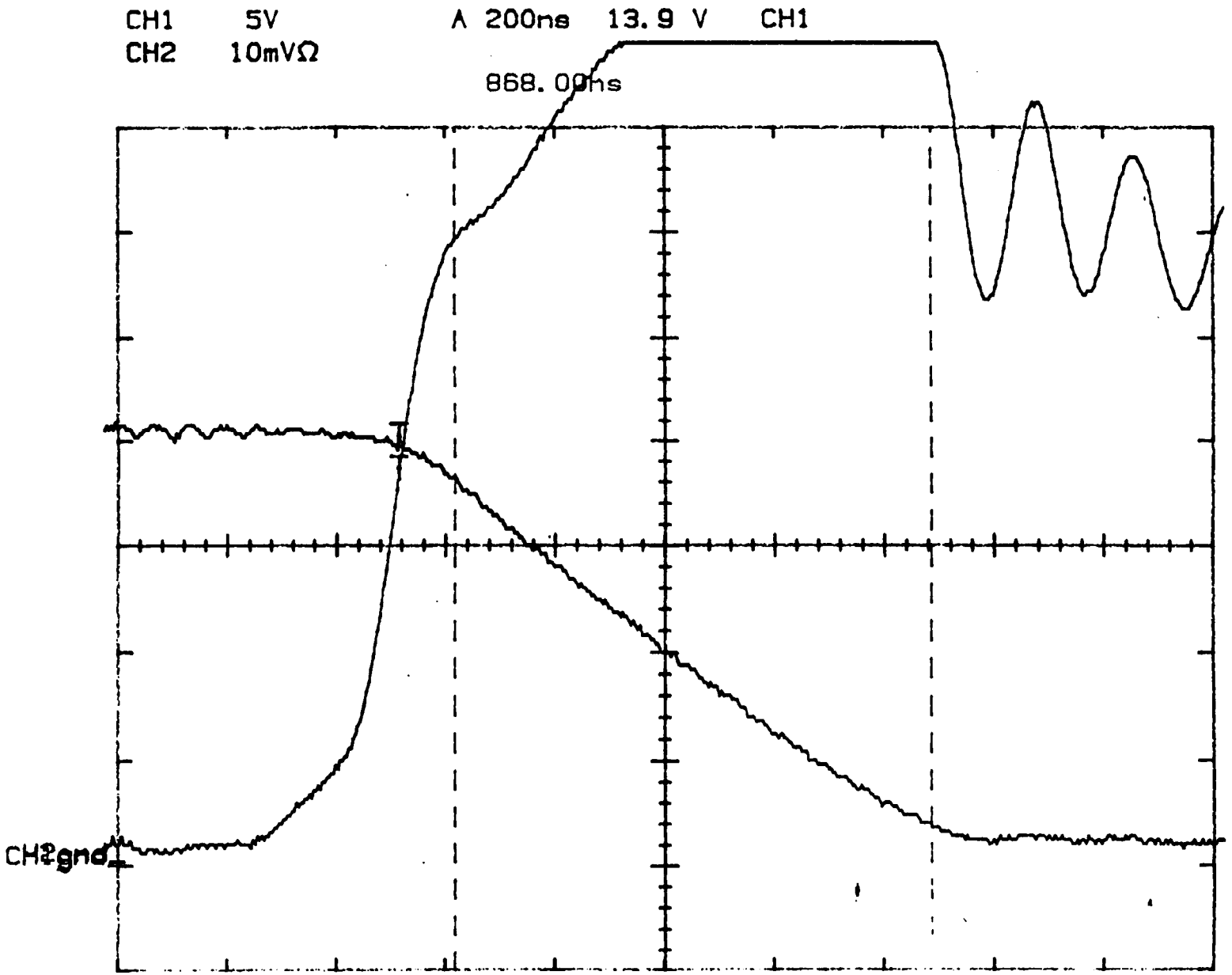

Figure 5. N-channel MOSFET turn off at 200°C.

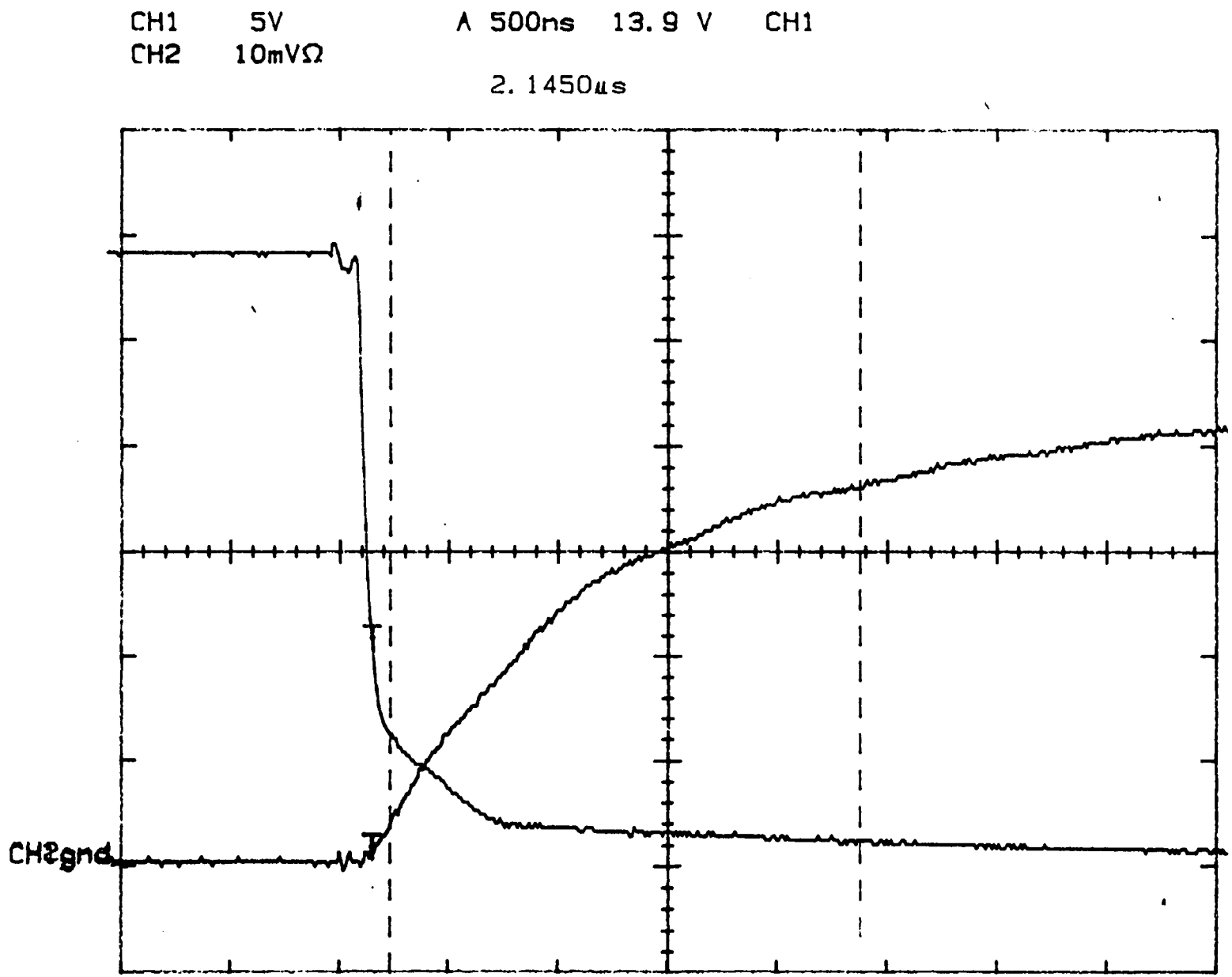

Figure 6. N-channel MOSFET turn on at 200°C.

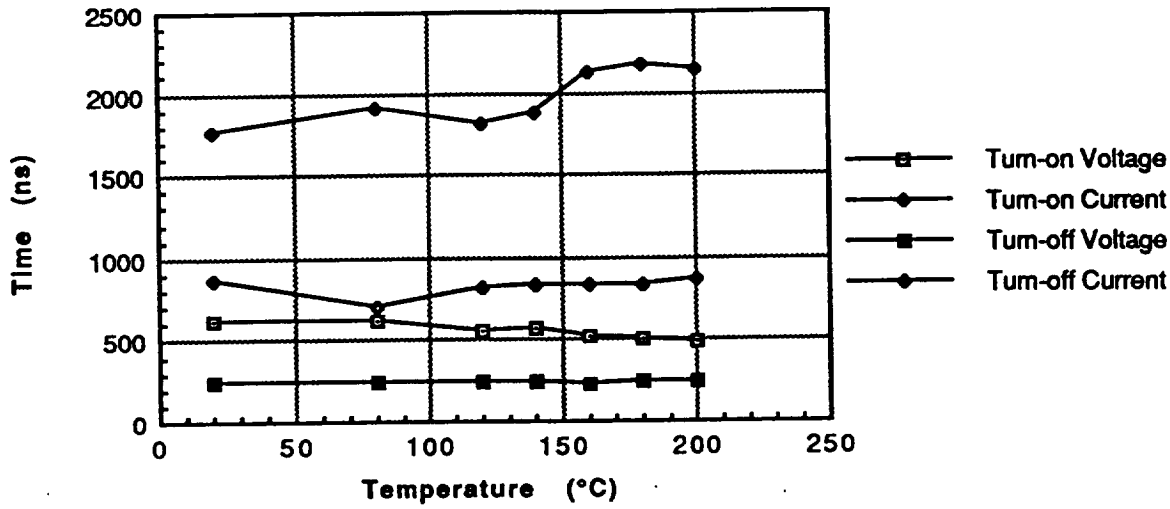

Figure 7. Resistive switching times for NMOS (RL=0.67Ω L=0.212μH).

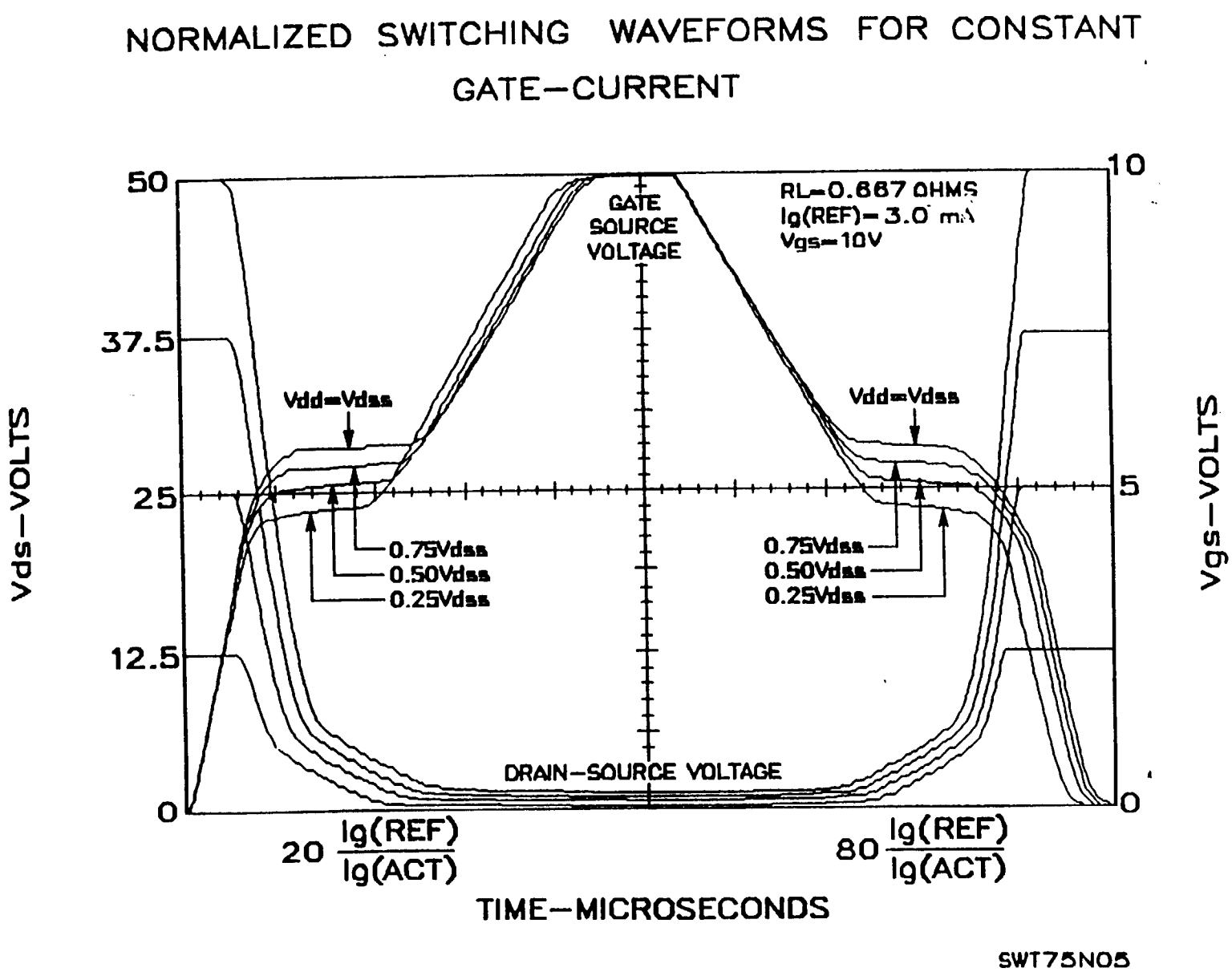

Figure 8. MOSFET charge transfer characteristics.

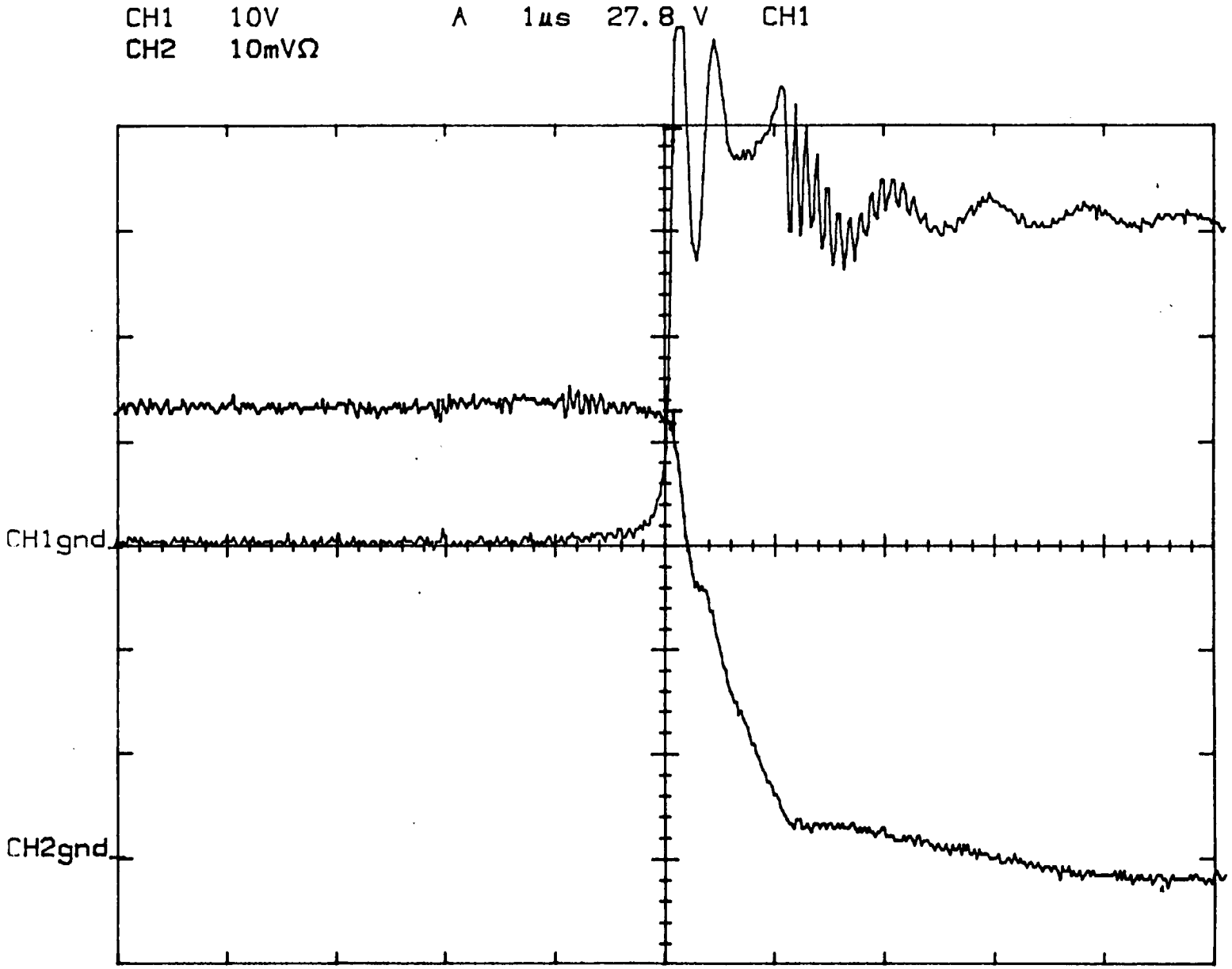

Figure 9. BJT turn off at 20°C.

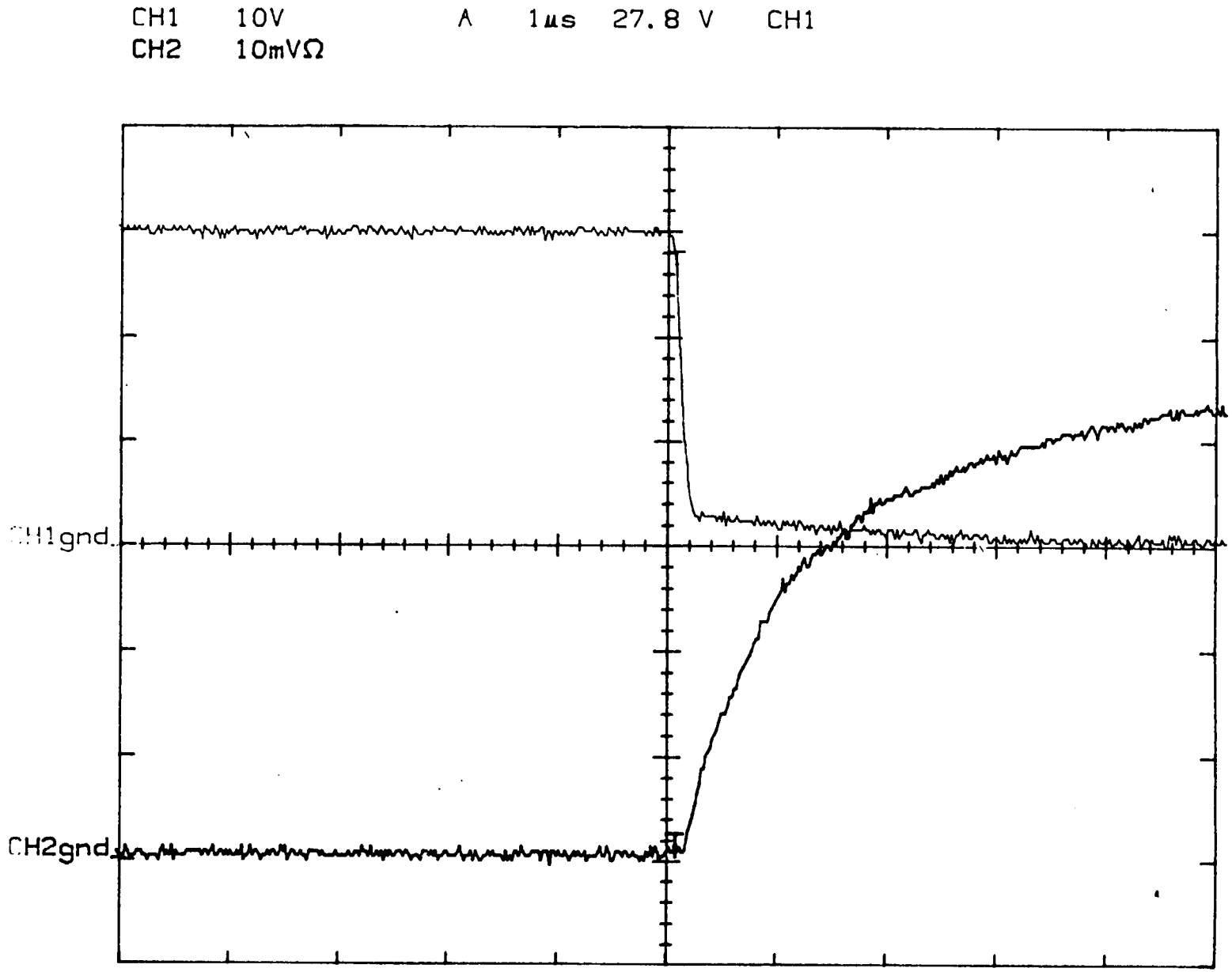

Figure 10. BJT turn on at 20°C.

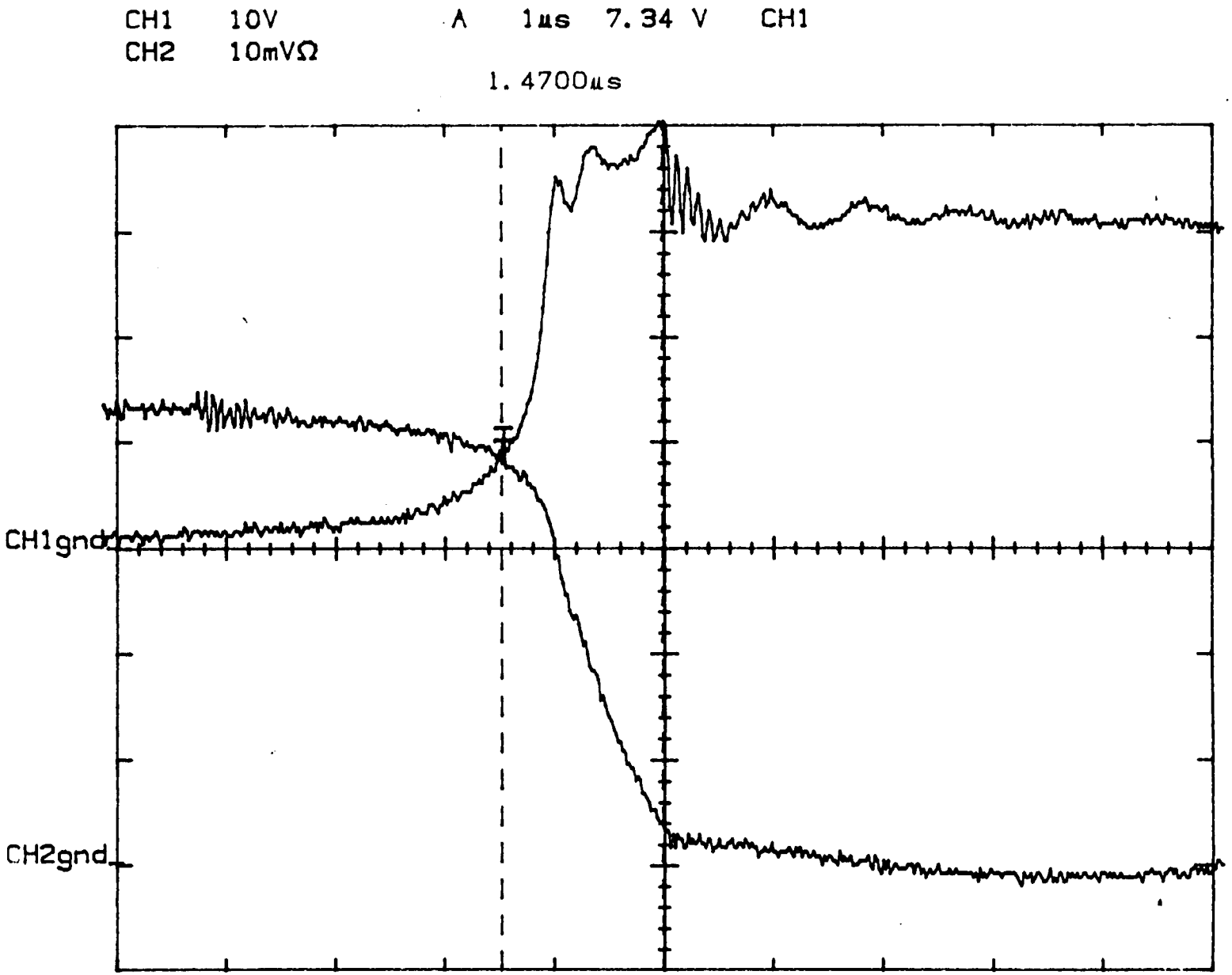

Figure 11. BJT turn off at 200°C.

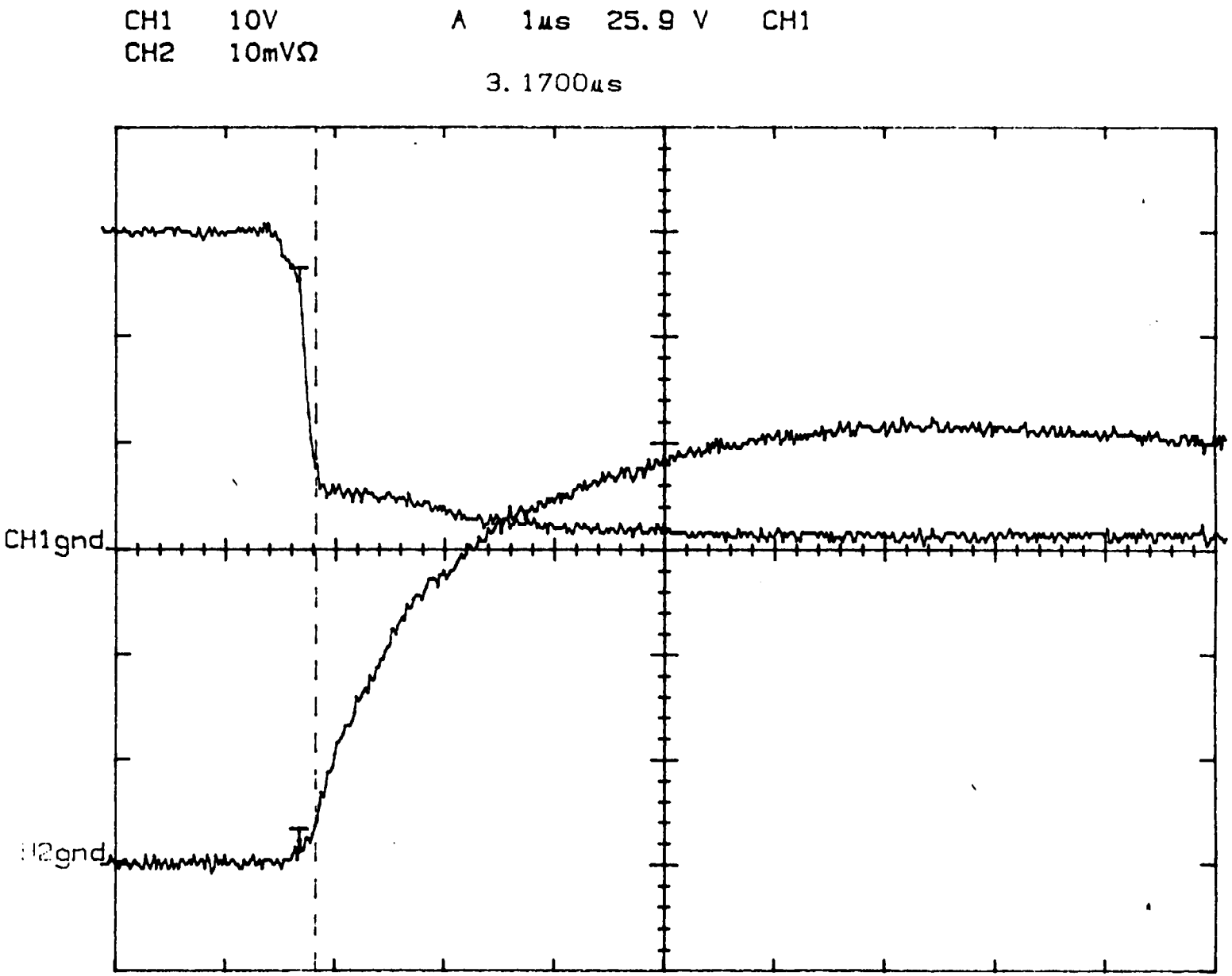

Figure 12. BJT turn on at 200°C.

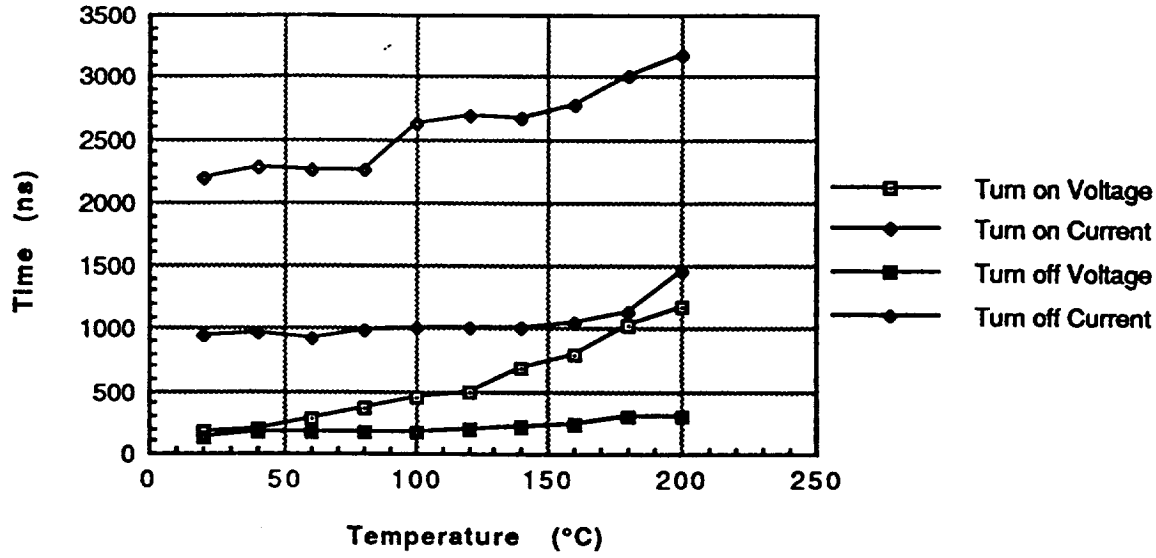

Figure 13. Resistive switching times for BJT (RL=0.67Ω L=0.212μH).

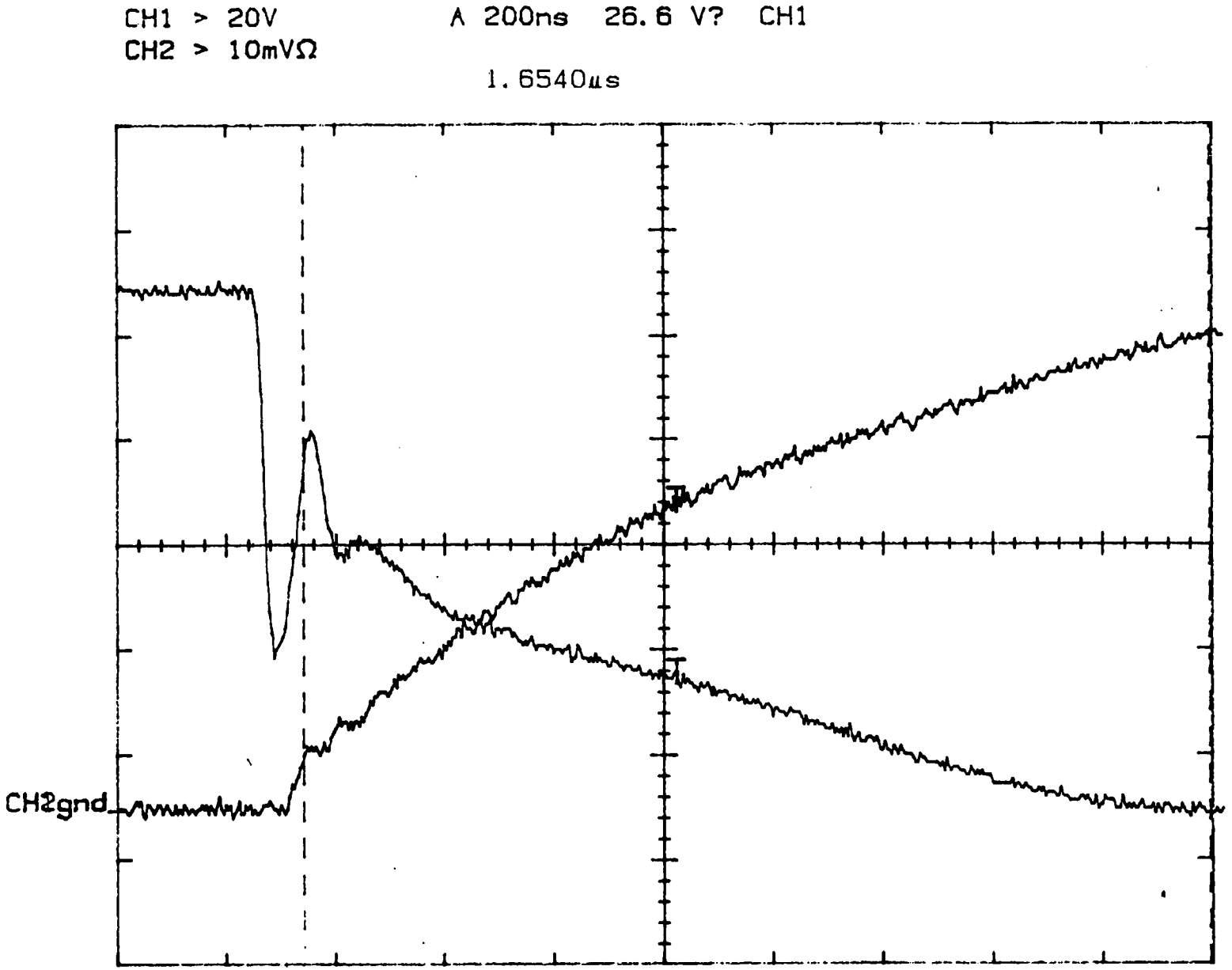

Figure 14. IGBT turn off at 20°C.

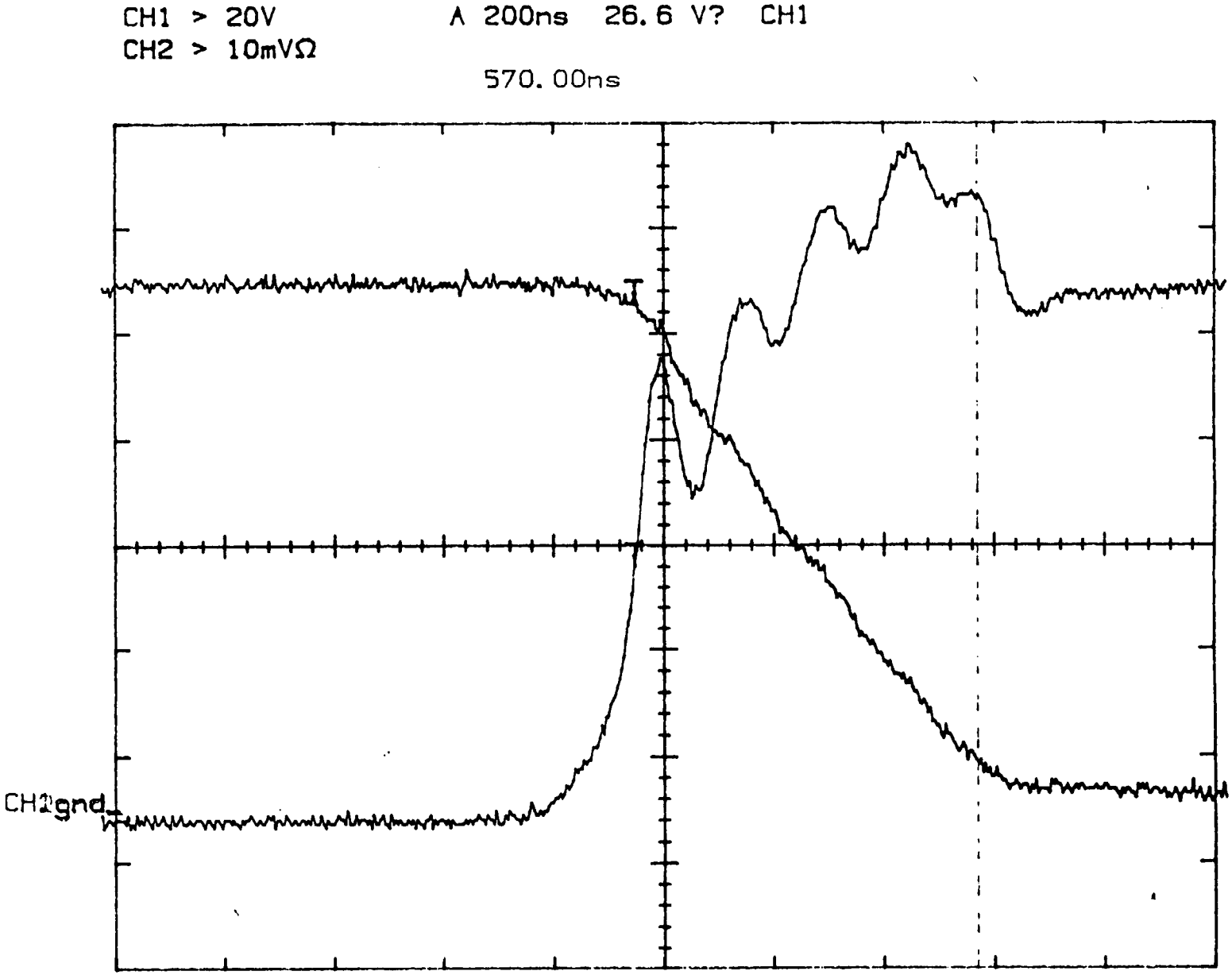

Figure 15. IGBT turn on at 20°C.

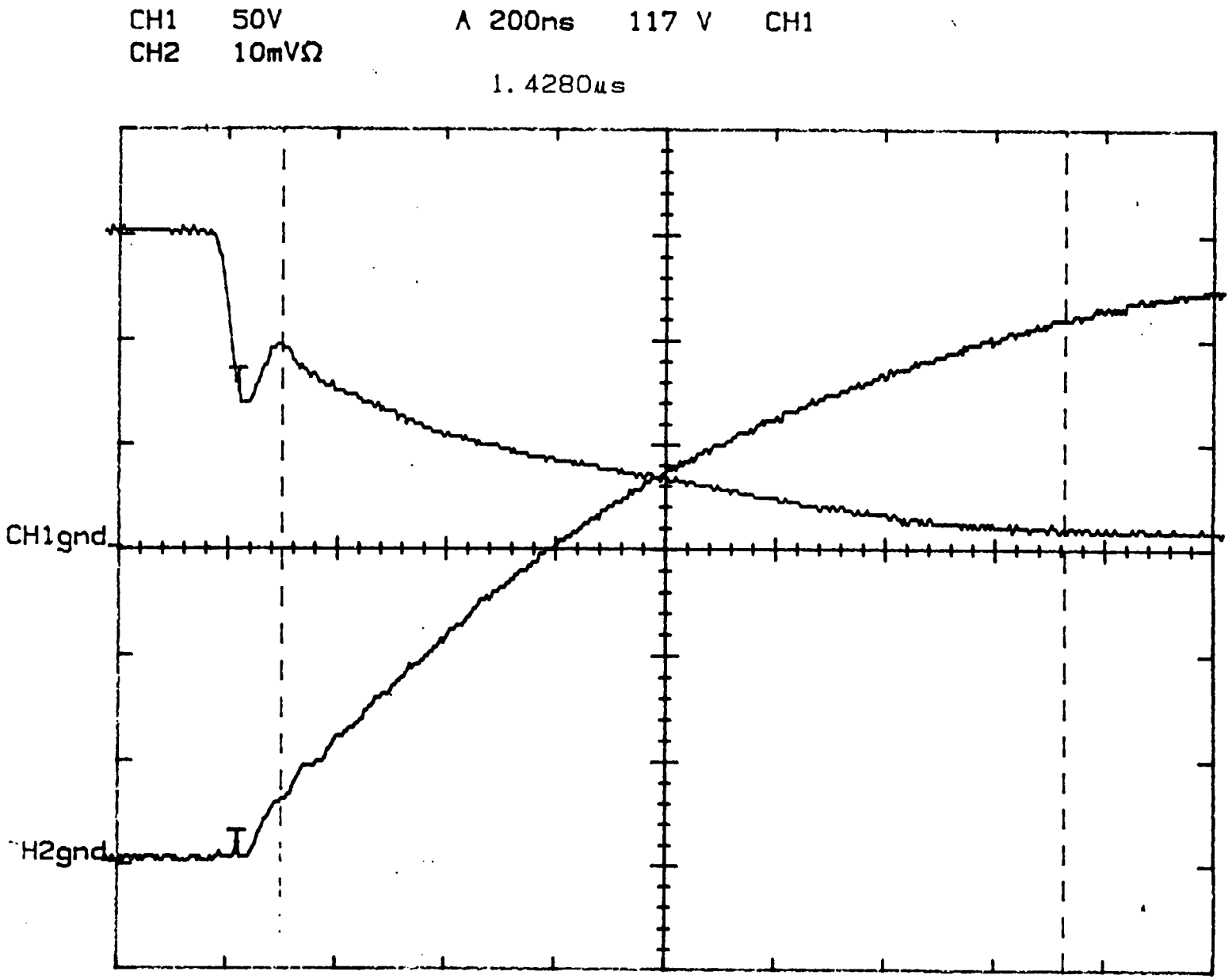

Figure 16. IGBT turn off at 200°C.

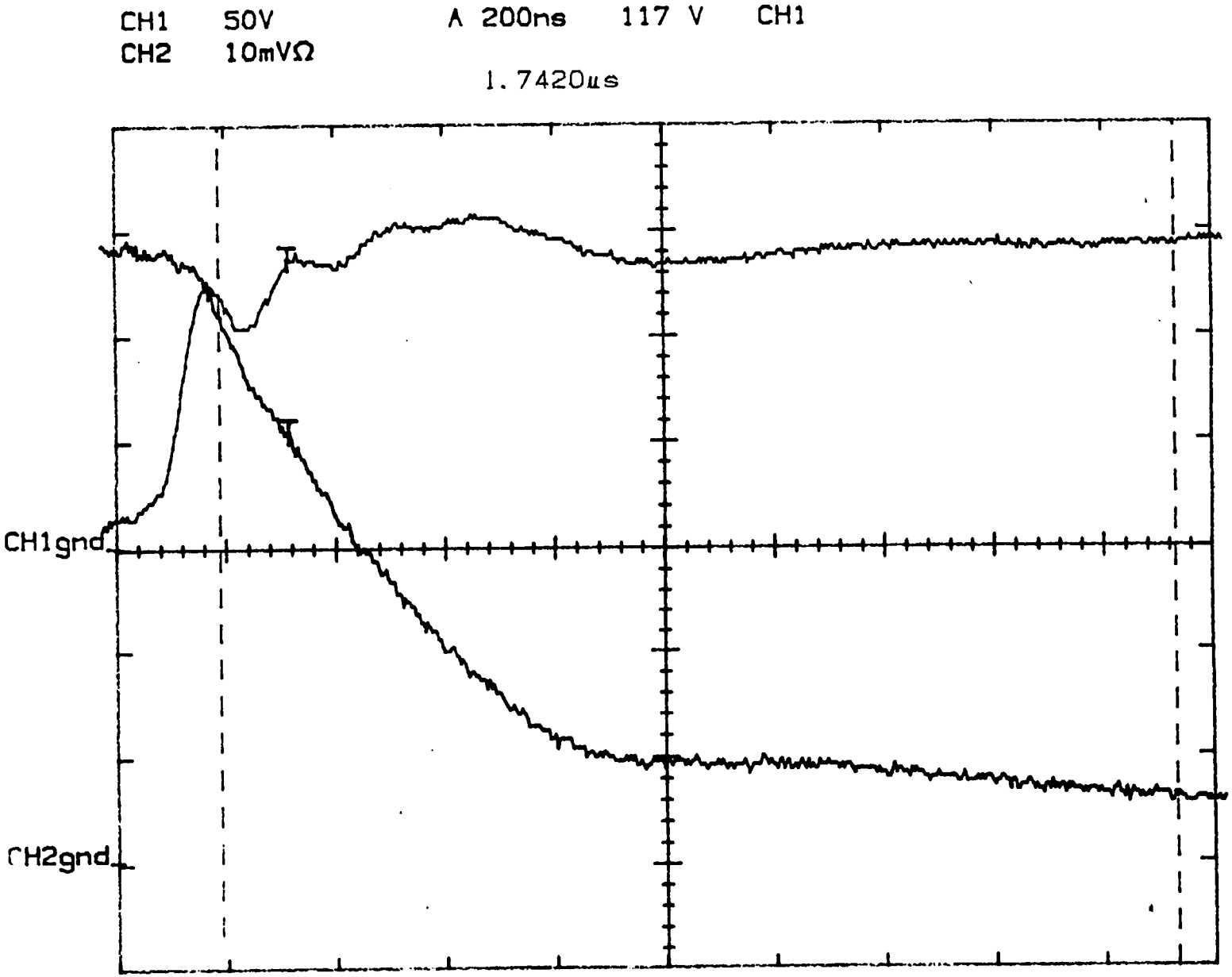

Figure 17. IGBT turn on at 200°C.

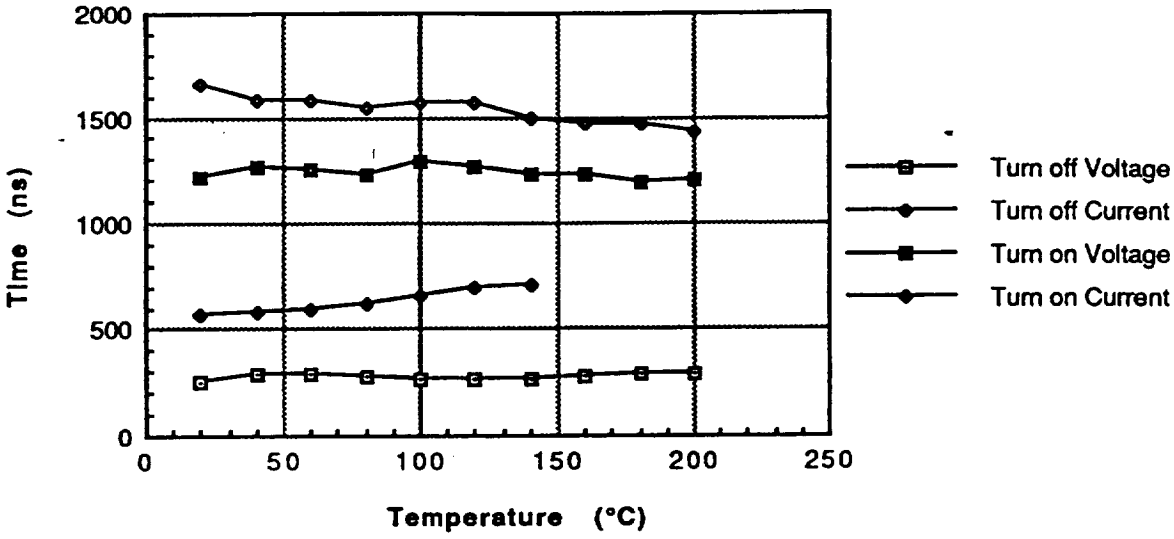

Figure 18. Resistive switching times for IGBT (RL=5.56Ω L=1.21μH).

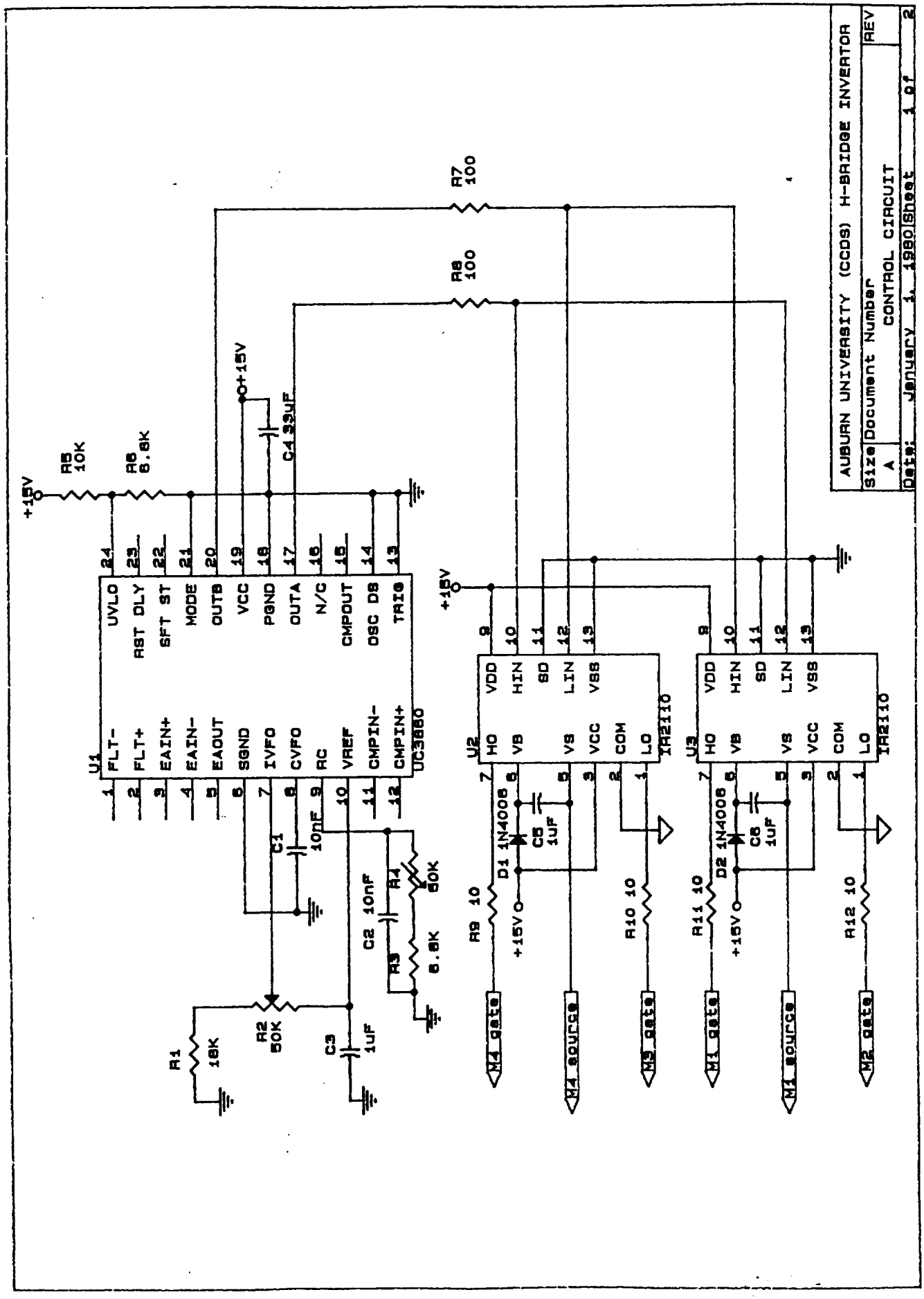

Figure 19. H-bridge control circuitry.

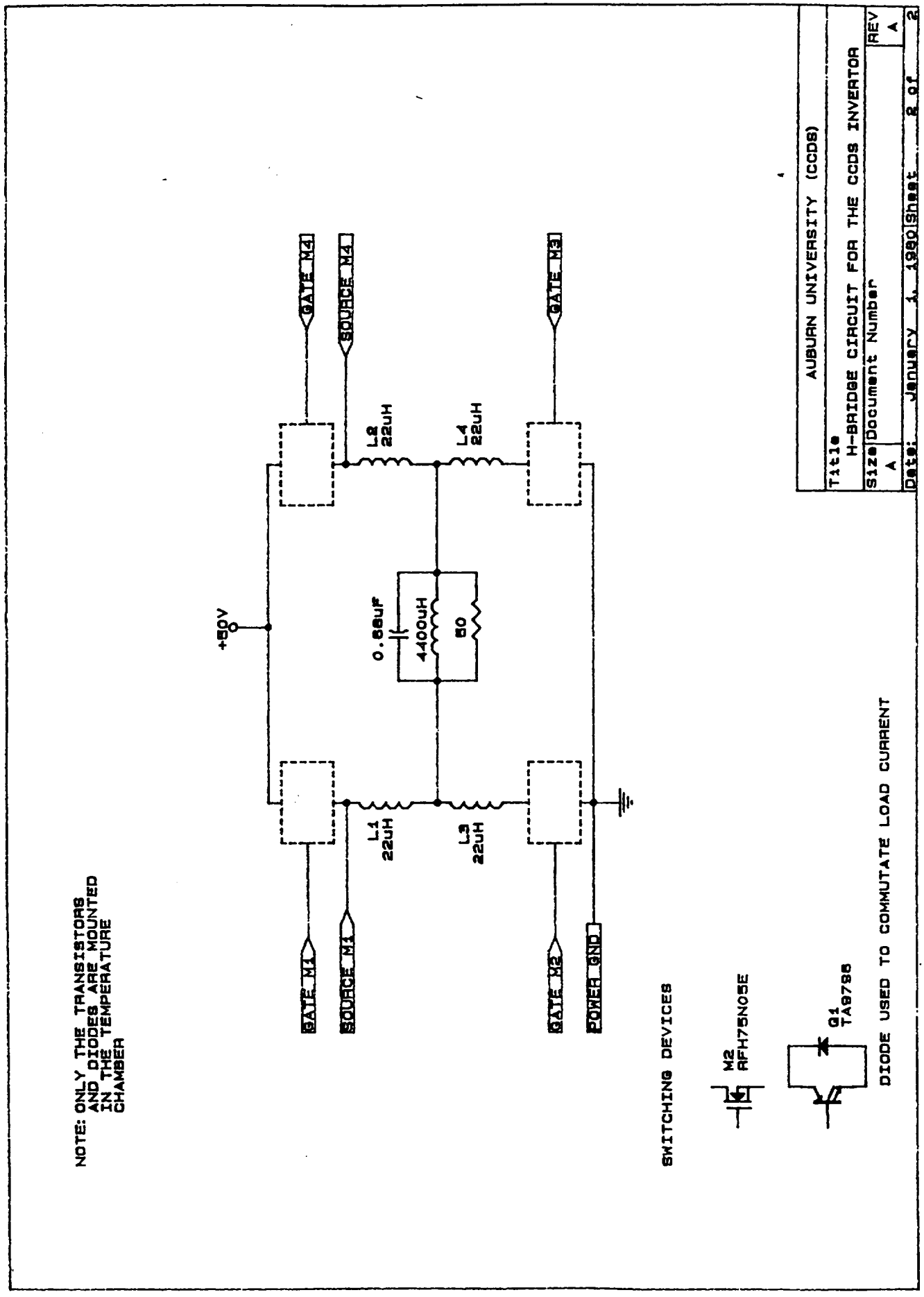

Figure 20. H-bridge schematic.

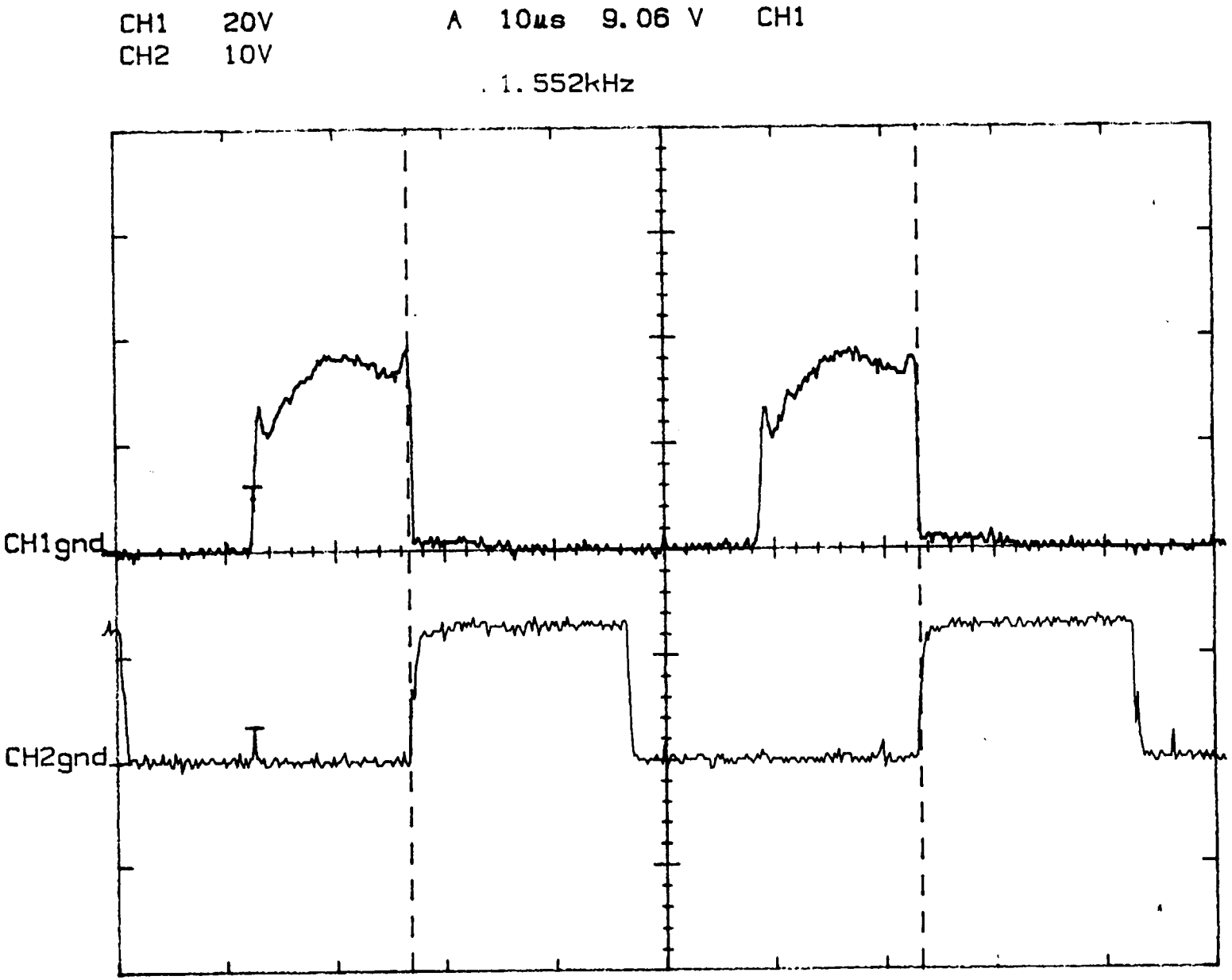

Figure 21. Vds and Vgs of low-side device, M3.

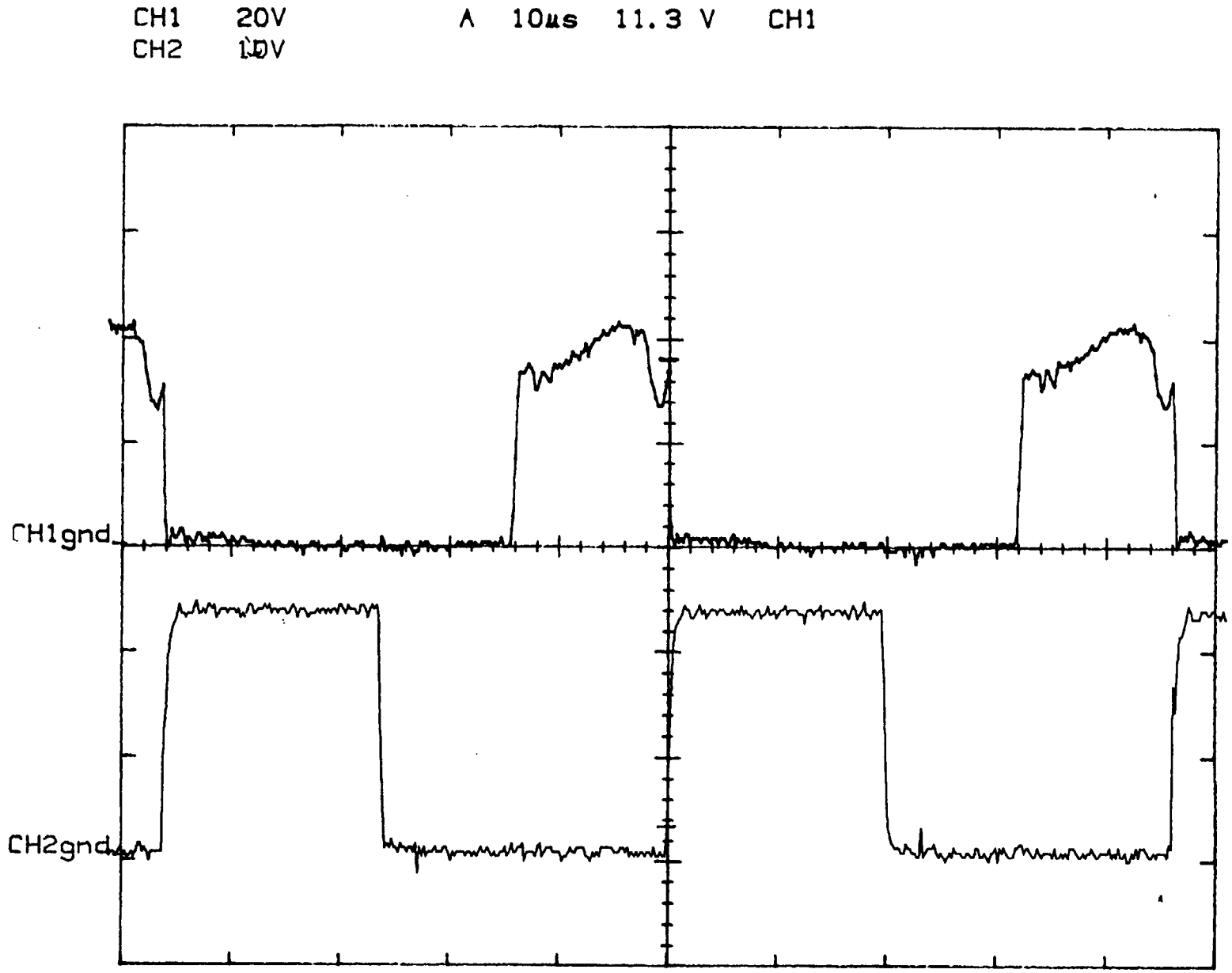

Figure 22. Vds and Vgs of high-side device, M4.

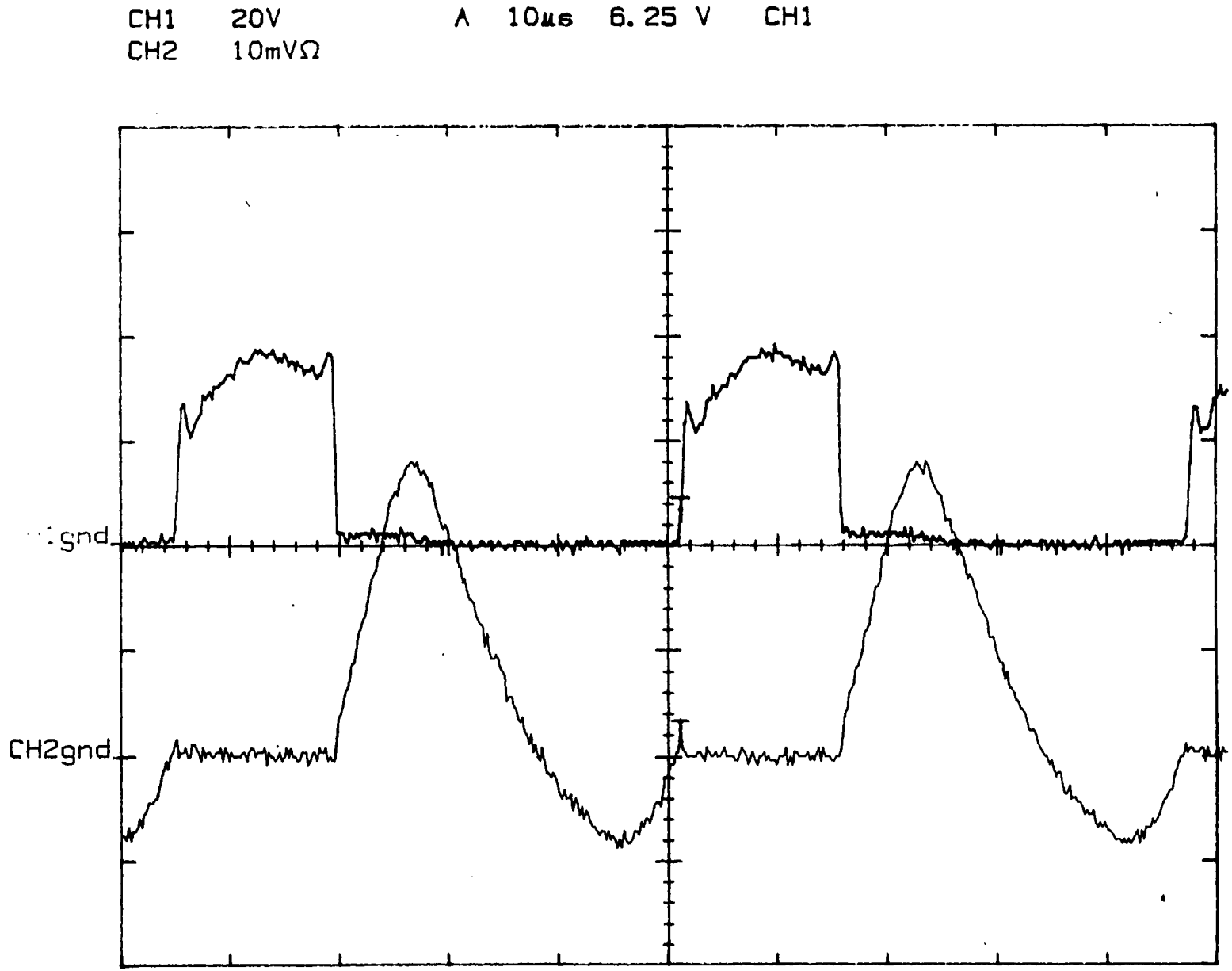

Figure 23. Vds and Id of low-side device, M3.

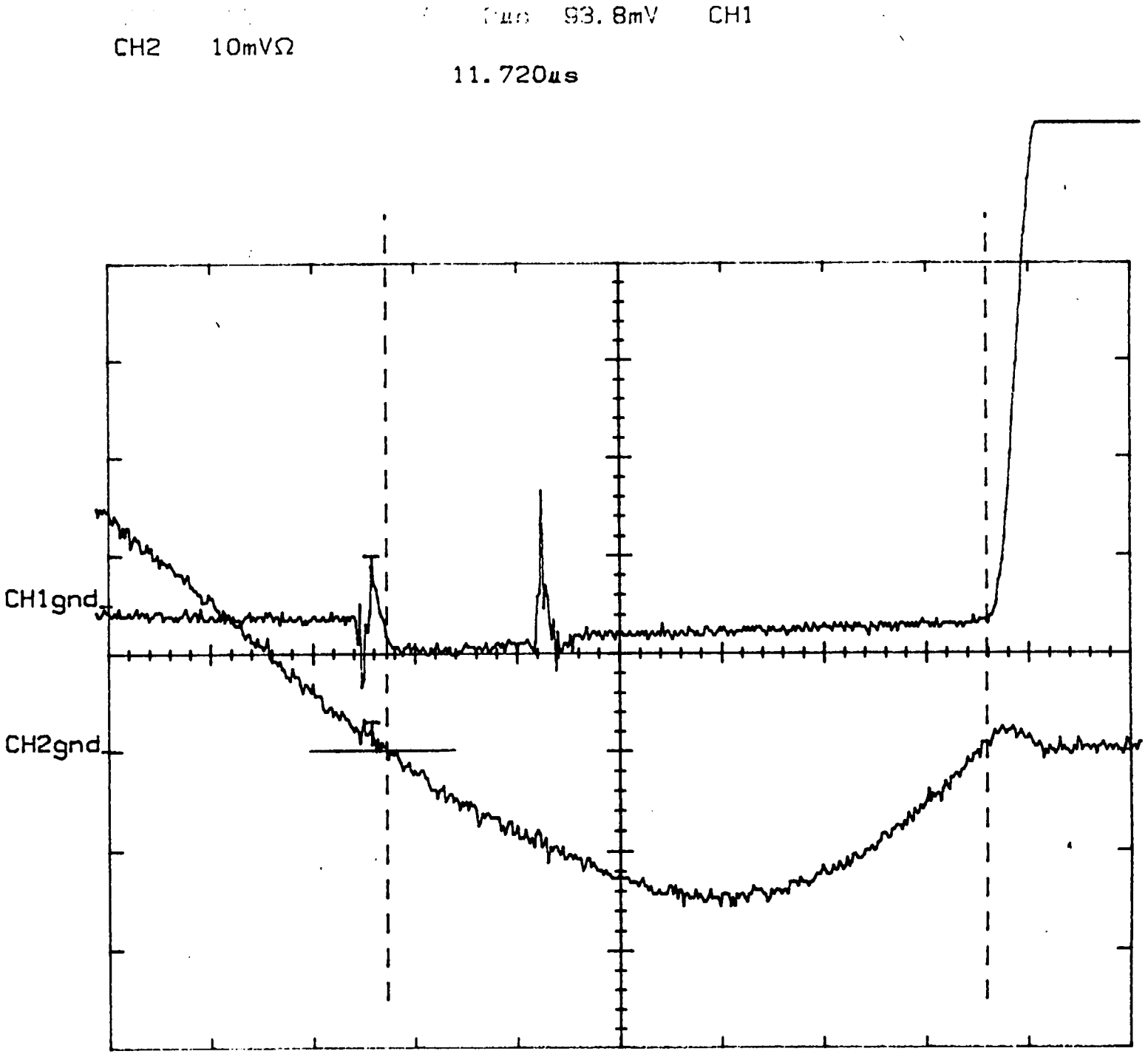

Figure 24. Forward conduction characteristic of body diode.

Figure 25. Optical photo of metalization failure in NMOS